

## CMOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

■ CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage ( $V_P$ ) and the negative voltage ( $V_N$ ) is defined as hysteresis voltage ( $V_H$ ) (see Fig. 2).

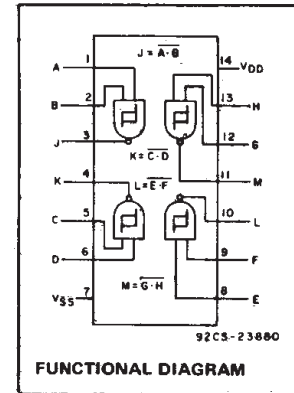
The CD4093 types are supplied in a 14-lead hermetic dual-in-line ceramic package (F suffix), 14-lead dual-in-line plastic package (E suffix), 14-lead dual-in-line plastic small-outline package (M), and in chip form (H suffix). Add the suffix 96 to the M package for tape and reel.

### Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at  $V_{DD} = 5$  V and 2.3 V at  $V_{DD} = 10$  V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



### RECOMMENDED OPERATING CONDITIONS

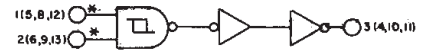
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range ( $T_A =$ Full Package Temp. Range)	3	18	V

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10$ mA
PACKAGE THERMAL IMPEDANCE, $\theta_{JA}$ (See Note 1):	
E package	80°C/W
M package	86°C/W
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	-55°C to +125°C
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	+265°C

NOTE 1: Package thermal impedance is calculated in accordance with JESD 51.



\* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

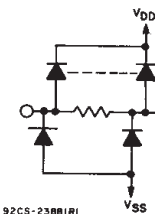


Fig. 1 - Logic diagram-1 of 4 Schmitt triggers.

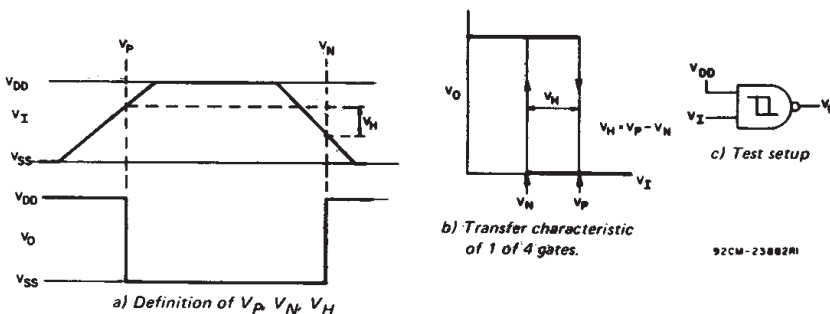


Fig. 2 - Hysteresis definition, characteristic, and test setup.

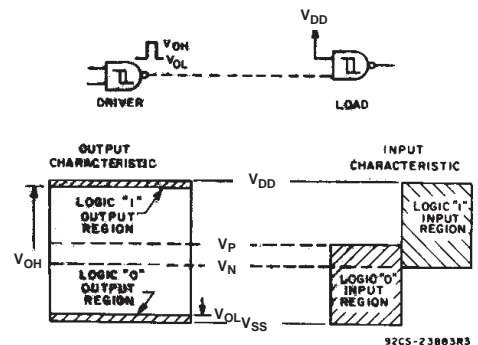


Fig. 3 - Input and output characteristics.

# CD4093B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								MIN.	TYP.	MAX.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0.5	5	1	1	30	30	-	0.02	1	μA
	-	0.10	10	2	2	60	60	-	0.02	2	
	-	0.15	15	4	4	120	120	-	0.02	4	
	-	0.20	20	20	20	600	600	-	0.04	20	
Positive Trigger Threshold Voltage V <sub>p</sub> Min.	-	a	5	2.2	2.2	2.2	2.2	2.2	2.9	-	V
	-	a	10	4.6	4.6	4.6	4.6	4.6	5.9	-	
	-	a	15	6.8	6.8	6.8	6.8	6.8	8.8	-	
	-	b	5	2.6	2.6	2.6	2.6	2.6	3.3	-	
	-	b	10	5.6	5.6	5.6	5.6	5.6	7	-	
	-	b	15	6.3	6.3	6.3	6.3	6.3	9.4	-	
V <sub>p</sub> Max.	-	a	5	3.6	3.6	3.6	3.6	-	2.9	3.6	V
	-	a	10	7.1	7.1	7.1	7.1	-	5.9	7.1	
	-	a	15	10.8	10.8	10.8	10.8	-	8.8	10.8	
	-	b	5	4	4	4	4	-	3.3	4	
	-	b	10	8.2	8.2	8.2	8.2	-	7	8.2	
	-	b	15	12.7	12.7	12.7	12.7	-	9.4	12.7	
Negative Trigger Threshold Voltage V <sub>N</sub> Min.	-	a	5	0.9	0.9	0.9	0.9	0.9	1.9	-	V
	-	a	10	2.5	2.5	2.5	2.5	2.5	3.9	-	
	-	a	15	4	4	4	4	4	5.8	-	
	-	b	5	1.4	1.4	1.4	1.4	1.4	2.3	-	
	-	b	10	3.4	3.4	3.4	3.4	3.4	5.1	-	
	-	b	15	4.8	4.8	4.8	4.8	4.8	7.3	-	
V <sub>N</sub> Max.	-	a	5	2.8	2.8	2.8	2.8	-	1.9	2.8	V
	-	a	10	5.2	5.2	5.2	5.2	-	3.9	5.2	
	-	a	15	7.4	7.4	7.4	7.4	-	5.8	7.4	
	-	b	5	3.2	3.2	3.2	3.2	-	2.3	3.2	
	-	b	10	6.6	6.6	6.6	6.6	-	5.1	6.6	
	-	b	15	9.6	9.6	9.6	9.6	-	7.3	9.6	
Hysteresis Voltage V <sub>H</sub> Min.	-	a	5	0.3	0.3	0.3	0.3	0.3	0.9	-	V
	-	a	10	1.2	1.2	1.2	1.2	1.2	2.3	-	
	-	a	15	1.6	1.6	1.6	1.6	1.6	3.5	-	
	-	b	5	0.3	0.3	0.3	0.3	0.3	0.9	-	
	-	b	10	1.2	1.2	1.2	1.2	1.2	2.3	-	
	-	b	15	1.6	1.6	1.6	1.6	1.6	3.5	-	
V <sub>H</sub> Max.	-	a	5	1.6	1.6	1.6	1.6	-	0.9	1.6	V
	-	a	10	3.4	3.4	3.4	3.4	-	2.3	3.4	
	-	a	15	5	5	5	5	-	3.5	5	
	-	b	5	1.6	1.6	1.6	1.6	-	0.9	1.6	
	-	b	10	3.4	3.4	3.4	3.4	-	2.3	3.4	
	-	b	15	5	5	5	5	-	3.5	5	

<sup>a</sup> Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to V<sub>DD</sub>.

<sup>b</sup> Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V<sub>DD</sub>.

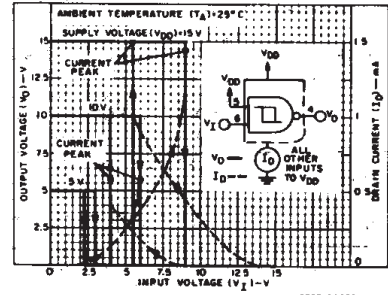


Fig. 4 - Typical current and voltage transfer characteristics.

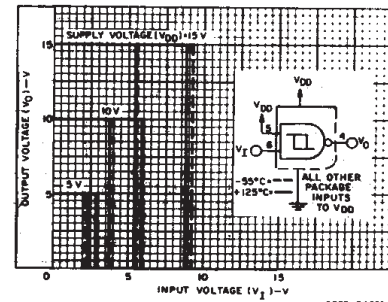


Fig. 5 - Typical voltage transfer characteristics as a function of temperature.

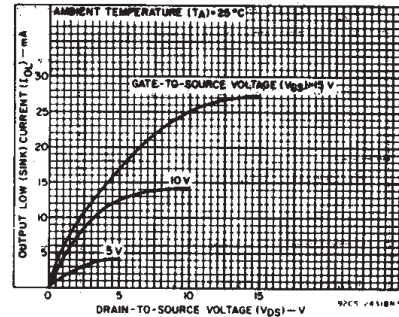


Fig. 6 - Typical output low (sink) current characteristics.

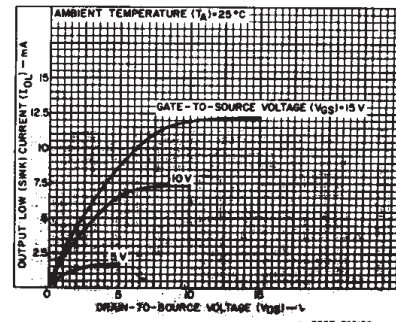


Fig. 7 - Minimum output low (sink) current characteristics.

# CD4093B Types

## STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								MIN.	TYP.	MAX.	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage Low-Level, V <sub>OL</sub> Max.	—	0.5	5	0.05				—	0	0.05	V
	—	0.10	10	0.05				—	0	0.05	
	—	0.15	15	0.05				—	0	0.05	
Output Voltage High-Level, V <sub>OH</sub> Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0.10	10	9.95				9.95	10	—	
	—	0.15	15	14.95				14.95	—	—	
Input Current, I <sub>IN</sub> Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

## DYNAMIC ELECTRICAL CHARACTERISTICS

At T<sub>A</sub> = 25°C; Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V <sub>DD</sub> VOLTS	TYP.	MAX.	
Propagation Delay Time: t <sub>PHL</sub> t <sub>PLH</sub>		5	190	380	ns
		10	90	180	
		15	65	130	
Transition Time, t <sub>THL</sub> t <sub>TLH</sub>		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C <sub>IN</sub>	Any Input		5	7.5	pF

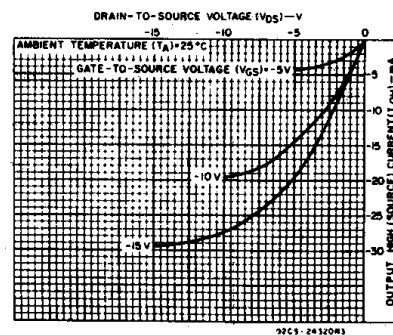


Fig. 8 – Typical output high (source) current characteristics.

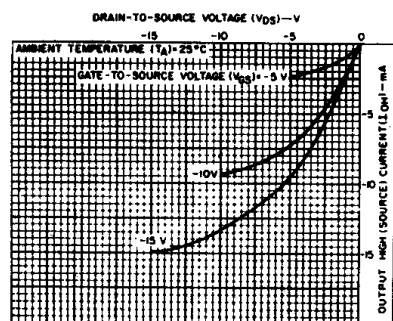


Fig. 9 – Minimum output high (source) current characteristics.

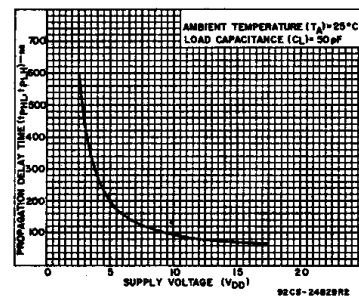


Fig. 10 – Typical propagation delay time vs. supply voltage.

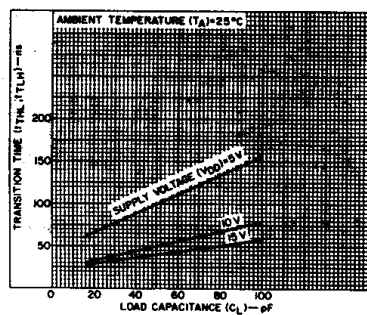


Fig. 11 – Typical transition time vs. load capacitance.

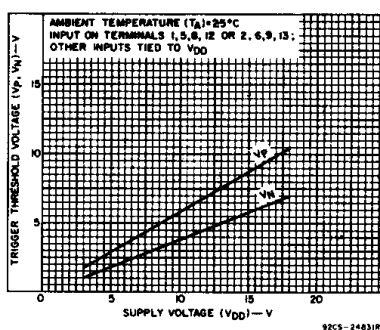


Fig. 12 – Typical trigger threshold voltage vs. V<sub>DD</sub>

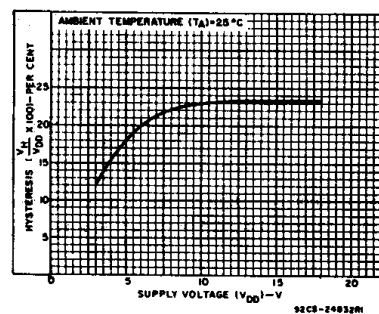


Fig. 13 – Typical per cent hysteresis vs. supply voltage.

# CD4093B Types

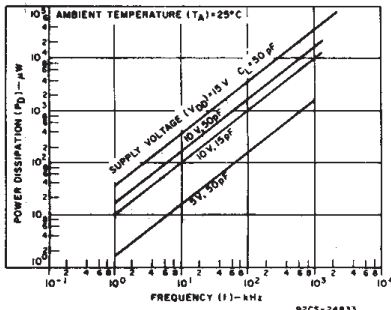


Fig. 14 - Typical power dissipation vs. frequency characteristics.

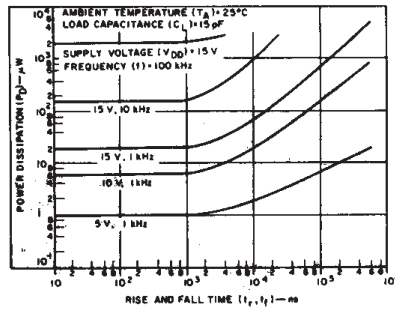


Fig. 15 - Typical power dissipation vs. rise and fall times.

## APPLICATIONS

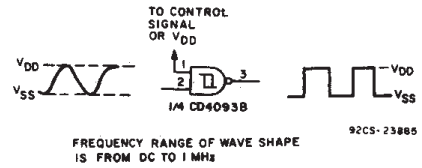


Fig. 16 - Wave shaper.

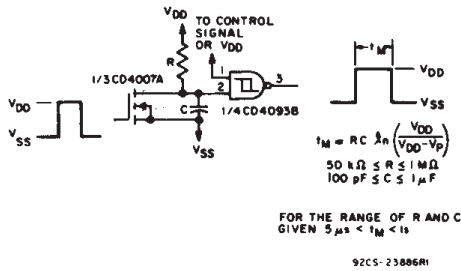


Fig. 17 - Monostable multivibrator.

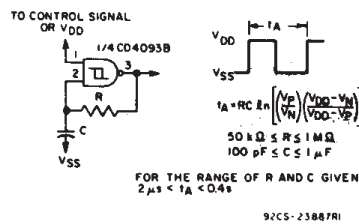


Fig. 18 - Astable multivibrator.

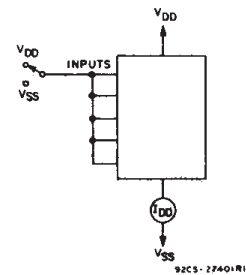


Fig. 19 - Quiescent device current test circuit.

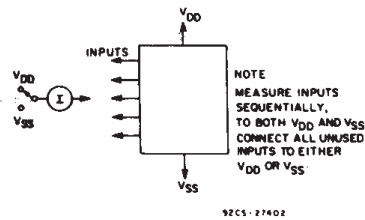
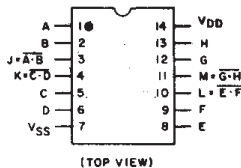


Fig. 20 - Input current test circuit.



TERMINAL ASSIGNMENT

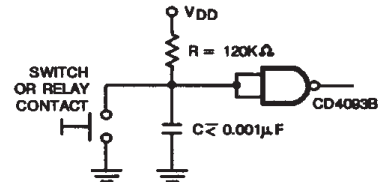


Fig. 21 - Contact Debouncer

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