

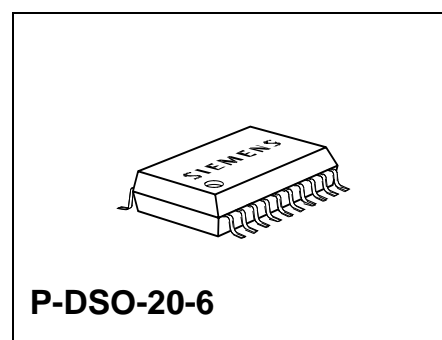
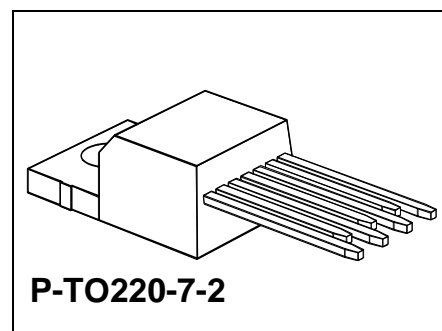
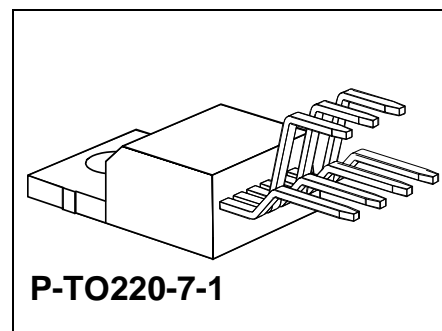
5-V Low-Drop Voltage Regulator

TLE 4261

Bipolar IC

Features

- Very low-drop voltage
- Very low quiescent current
- Low starting-current consumption
- Proof against reverse polarity
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- External setting of reset delay
- Integrated watchdog circuit
- Wide temperature range
- Overtemperature protection
- Suitable for automotive use
- EMC proofed (100 V/m)



Type	Ordering Code	Package
▼ TLE 4261	Q67000-A9003	P-TO220-7-1
▼ TLE 4261 S	Q67000-A9109	P-TO220-7-2
▼ TLE 4261 G	Q67000-A9059	P-DSO-20-6 (SMD)

▼ Please also refer to the new pin compatible device TLE 4271

Functional Description

TLE 4261 is a 5-V low-drop voltage regulator in a P-TO220-7 or in a P-DSO package. The maximum input voltage is 42 V (65 V/ ≤ 400 ms). The device can produce an output current of more than 500 mA. It is short-circuit proof and incorporates temperature protection that disables the circuit at impermissibly high temperatures.

Application Description

The IC regulates an input voltage V_I in the range $V_I = 6\text{ V}$ to 40 V to $V_{Q\text{rated}} = 5.0\text{ V}$. A reset signal is generated for a maximum output voltage of V_Q less than 4.75 V . The reset delay can be set externally with a capacitor. A connected microprocessor is monitored by the integrated watchdog circuit. Connecting this input to the input voltage makes the watchdog function inactive. The presence of a voltage less than 2 V on inhibit input disables the regulator. The current consumption drops to max. $50\text{ }\mu\text{A}$.

Design Notes for External Components

The input capacitor C_I causes a low-resistance powerline and limits the rise times of the input voltage. The IC is protected against rise times up to $100\text{ V}/\mu\text{s}$. It is possible to damp the tuned circuit consisting of supply inductance and input capacitance with a resistor of approx. $1\text{ }\Omega$ in series to C_I .

The output capacitor maintains the stability of the regulating loop. Stability is guaranteed with a rating of $22\text{ }\mu\text{F}$ at an ESR of $3\text{ }\Omega$ max. in the operating temperature range.

Circuit Description

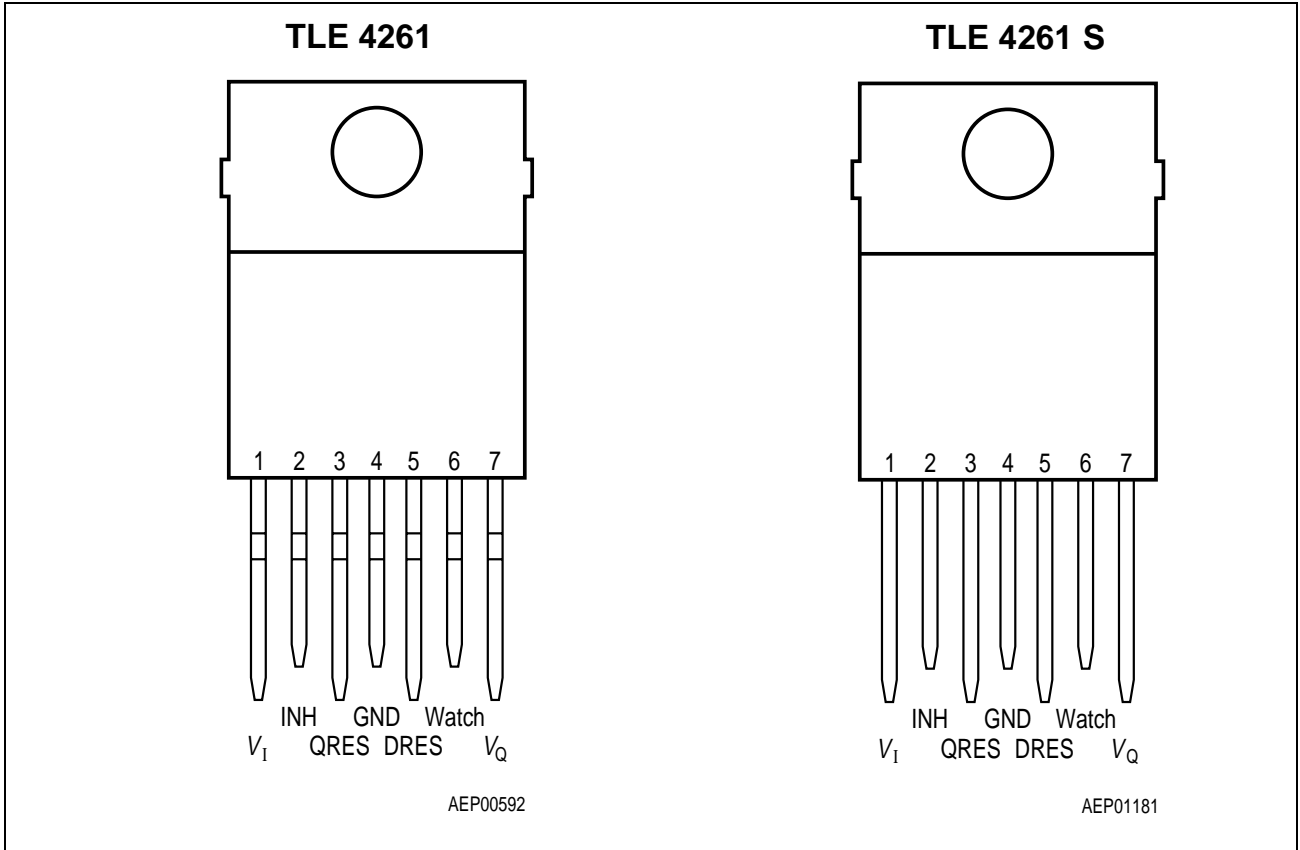
The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and controls the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage drops below 95.5% of its typical value for more than $2\text{ }\mu\text{s}$, a reset signal is triggered on pin 3 and an external capacitor is discharged on pin 5. The reset signal is not cancelled until the voltage on the capacitor has exceeded the upper switching threshold V_{DT} . A positive-edge-triggered watchdog circuit monitors the connected microprocessor and will likewise trigger a reset if pulses are missing. The IC can be disabled by a low level on the inhibit input and the current consumption drops to $< 50\text{ }\mu\text{A}$.

The IC also incorporates a number of circuits for protection against:

- Overload
- Overvoltage
- Overtemperature
- Reverse polarity

Pin Configuration

(top view)

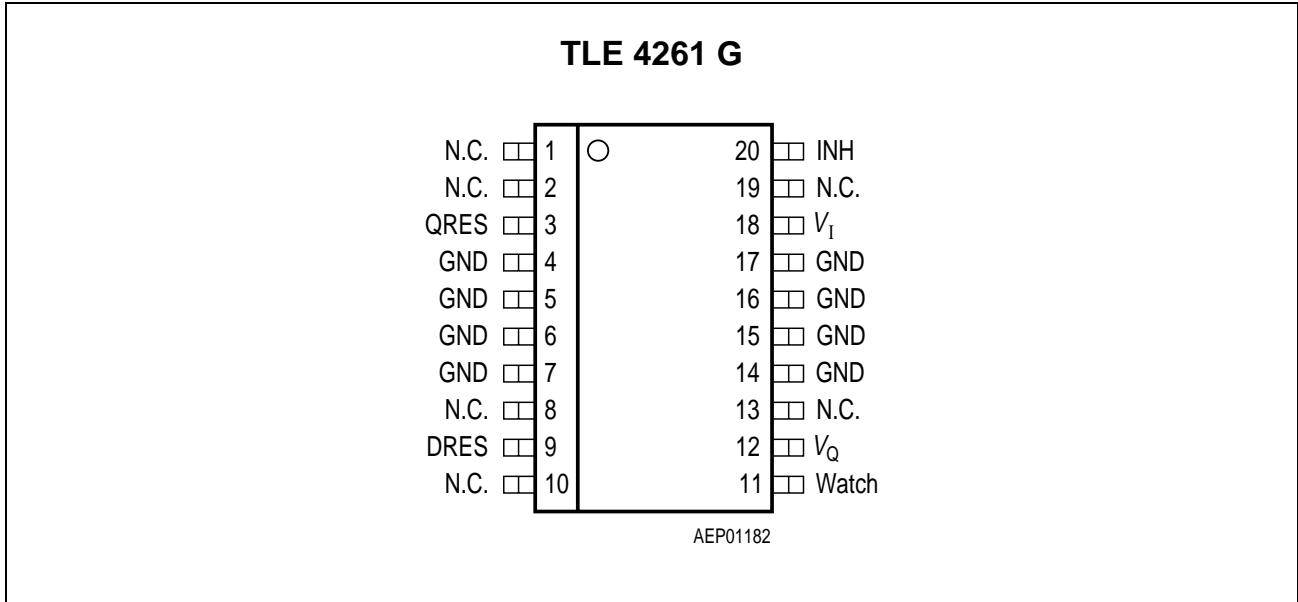


Pin Definitions and Functions (TLE 4261; S)

Pin	Symbol	Function
1	V_I	Input voltage; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vehicle electrical system. Oscillation of the input voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
2	INH	Inhibit; switches off the IC when low.
3	QRES	Reset output; open-collector output controlled by the rese delay.
4	GND	Ground
5	DRES	Reset delay; wired to ground using a capacitor.
6	Watch	Watchdog; monitors the microprocessor when active.
7	V_Q	5-V output voltage; block to ground using a capacitor of $\geq 22 \mu\text{F}$. ESR is $\leq 3 \Omega$ in the operating temperature range.

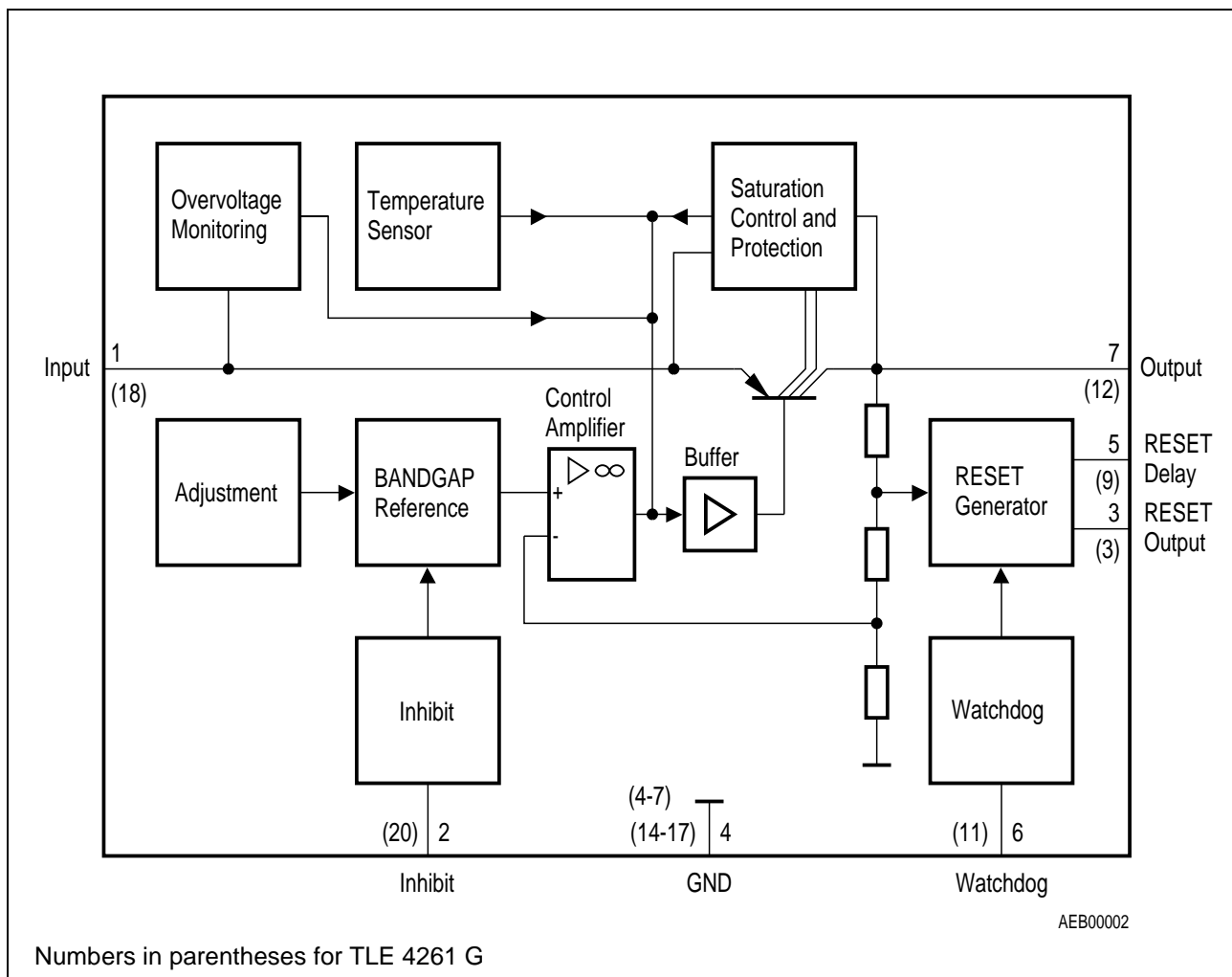
Pin Configuration

(top view)



Pin Definitions and Functions (TLE 4261 G)

Pin	Symbol	Function
18	V_I	Input voltage ; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vehicle electrical system. Oscillation of the input voltage can be damped by a resistor of approx. 1Ω in series with the input capacitor.
20	INH	Inhibit ; switches off the IC when low.
3	QRES	Reset output ; open-collector output controlled by the reset delay.
4 - 7 14 - 17	GND	Ground ; internally connected with pins 14 to 17.
9	DRES	Reset delay ; wired to ground using a capacitor.
11	Watch	Watchdog ; monitors the microprocessor when active.
12	V_Q	5-V output voltage ; block to ground using a capacitor of $\geq 22 \mu\text{F}$. ESR is $\leq 3 \Omega$ in the operating temperature range.
1, 2, 8, 10, 13, 19	N.C.	Not connected



Numbers in parentheses for TLE 4261 G

Block Diagram

Absolute Maximum Ratings

$T_j = -40$ to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Input

Input voltage	V_I	-42	45	V	-
Input voltage	V_I	-	65	V	$t \leq 400$ ms
Input current	I_I	-	1.6	A	-

Inhibit

Voltage	V_2	-0.3	42	V	-
Current	I_2	-	5	mA	-

Reset Output

Voltage	V_R	-0.3	42	V	-
Current	I_R	-	-	-	limited internally

Ground

Current	I_{GND}	-	0.5	A	-
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Reset Delay

Voltage	V_D	-0.3	42	V	-
Current	I_D	-	-	-	limited internally

Watchdog

Voltage	V_W	-0.3	V_I	V	-
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Output

Differential voltage	$V_I - V_Q$	-5.25	V_I	V	-
Current	I_Q	-	1.4	A	-

Absolute Maximum Ratings (cont'd)

$T_j = -40$ to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Temperature

Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Operating Range

Input voltage	V_i	–	32	V	see diagram
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistances

System-air	$R_{th SA}$	–	65 (70) ¹⁾	K/W	–
System-case	$R_{th SC}$	–	3 (15) ¹⁾	K/W	–

¹⁾ Figures in parenthesis refer to TLE 4261 G.

Characteristics

$V_1 = 13.5 \text{ V}$; $T_j = 25 \text{ °C}$; $V_2 \geq 6 \text{ V}$; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Normal Operation

Output voltage	V_Q	4.75	5.00	5.25	V	$25 \text{ mA} \leq I_Q \leq 500 \text{ mA}$; $6 \text{ V} \leq V_1 \leq 28 \text{ V}$; $-40 \text{ °C} \leq T_j \leq 125 \text{ °C}$
Output voltage	V_Q	4.85	5.00	5.15	V	$25 \text{ mA} \leq I_Q \leq 150 \text{ mA}$ $6 \text{ V} \leq V_1 \leq 40 \text{ V}$
Output current	I_Q	–	–	50	μA	$0 \text{ V} \leq V_1 \leq 2 \text{ V}$; $V_2 = V_1$; $-40 \text{ °C} \leq T_j \leq 125 \text{ °C}$
Output current	I_Q	500	1000	–	mA	$V_1 = 17 \text{ V to } 28 \text{ V}$
Current consumption; $I_q = I_1 - I_Q$	I_q	–	–	3.5	mA	$I_Q = 0$; $V_W > 6 \text{ V}$
Current consumption; $I_q = I_1 - I_Q$	I_q	–	5.0	10	mA	$6 \text{ V} \leq V_1 \leq 28 \text{ V}$ $I_Q = 150 \text{ mA}$
Current consumption; $I_q = I_1 - I_Q$	I_q	–	40	65	mA	$6 \text{ V} \leq V_1 \leq 28 \text{ V}$ $I_Q = 500 \text{ mA}$
Current consumption; $I_q = I_1 - I_Q$	I_q	–	45	80	mA	$V_1 < 6 \text{ V}$; $I_Q \leq 500 \text{ mA}$;
Drop voltage	V_{Dr}	–	0.35	0.5	V	$V_1 = 4.5 \text{ V}$; $I_Q = 0.5 \text{ A}$
Drop voltage	V_{Dr}	–	0.2	0.3	V	$V_1 = 4.5 \text{ V}$; $I_Q = 0.15 \text{ A}$
Load regulation	ΔV_Q	–	15	35	mV	$25 \text{ mA} \leq I_Q \leq 500 \text{ mA}$
Supply voltage regulation	ΔV_Q	–	15	50	mV	$6 \text{ V} \leq V_1 \leq 28 \text{ V}$ $I_Q = 100 \text{ mA}$
Supply voltage regulation	ΔV_Q	–	5	25	mV	$6 \text{ V} \leq V_1 \leq 16 \text{ V}$ $I_Q = 100 \text{ mA}$

Characteristics (cont'd)

$V_1 = 13.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; $V_2 \geq 6 \text{ V}$; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ripple rejection	SVR	–	54	–	dB	$f_r = 100 \text{ Hz}$; $V_r = 0.5 \text{ V}_{pp}$
Temperature drift of output voltage	α_{VQ}	–	2×10^{-4}	–	$1/^\circ\text{C}$	$-40 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$

Inhibit Operation

Current consumption	I_1	–	–	50	μA	$V_2 < 2 \text{ V}$; $I_Q = 0$
Current consumption	I_2	–	–	100	μA	$V_2 = 6 \text{ V}$
Switching threshold for inhibit	V_2	5.0	5.5	6.0	V	IC turned ON
Switching threshold for inhibit	V_2	2.0	2.7	3.7	V	IC turned OFF

Reset Generator

Switching threshold	V_{RT}	94	95.5	97	%	in % of V_Q $I_Q > 500 \text{ mA}$; $V_1 = 6 \text{ V}$
Saturation voltage, reset output	V_R	–	0.25	0.40	V	$I_R = 1 \text{ mA}$
Reverse current	I_R	–	–	1	μA	$V_R = 5 \text{ V}$
Charge current	I_d	18.75	25	31.25	μA	$V_C = 1.5 \text{ V}$
Switching threshold	V_{ST}	0.9	1	1.1	V	–
Delay switching threshold	V_{DT}	2.25	2.50	2.75	V	–
Saturation voltage, delay output	V_C	–	–	100	mV	$V_1 = 4.5 \text{ V}$ and I_d

Characteristics (cont'd)

$V_1 = 13.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; $V_2 \geq 6 \text{ V}$; (unless specified otherwise)

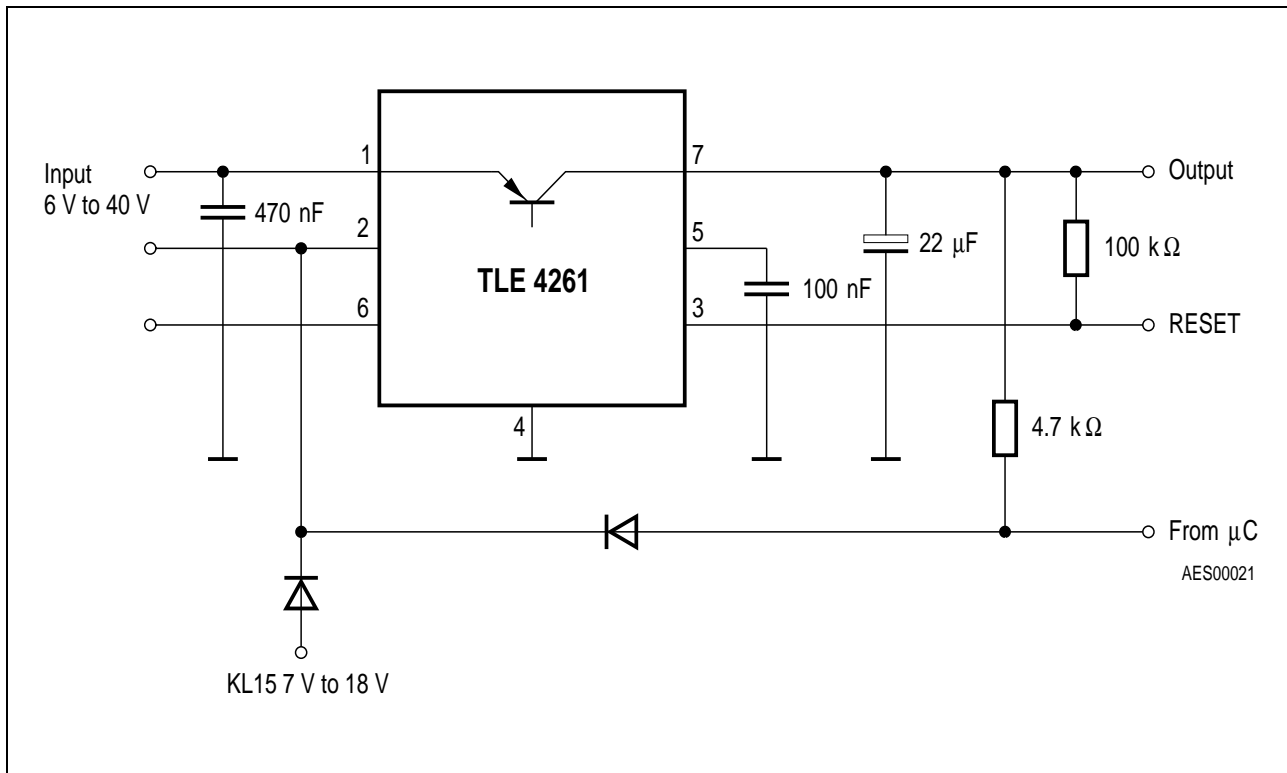
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay time	t_D	–	10	–	ms	$C_D = 100 \text{ nF}$
Delay time	t_t	–	2	–	μs	–

Watchdog

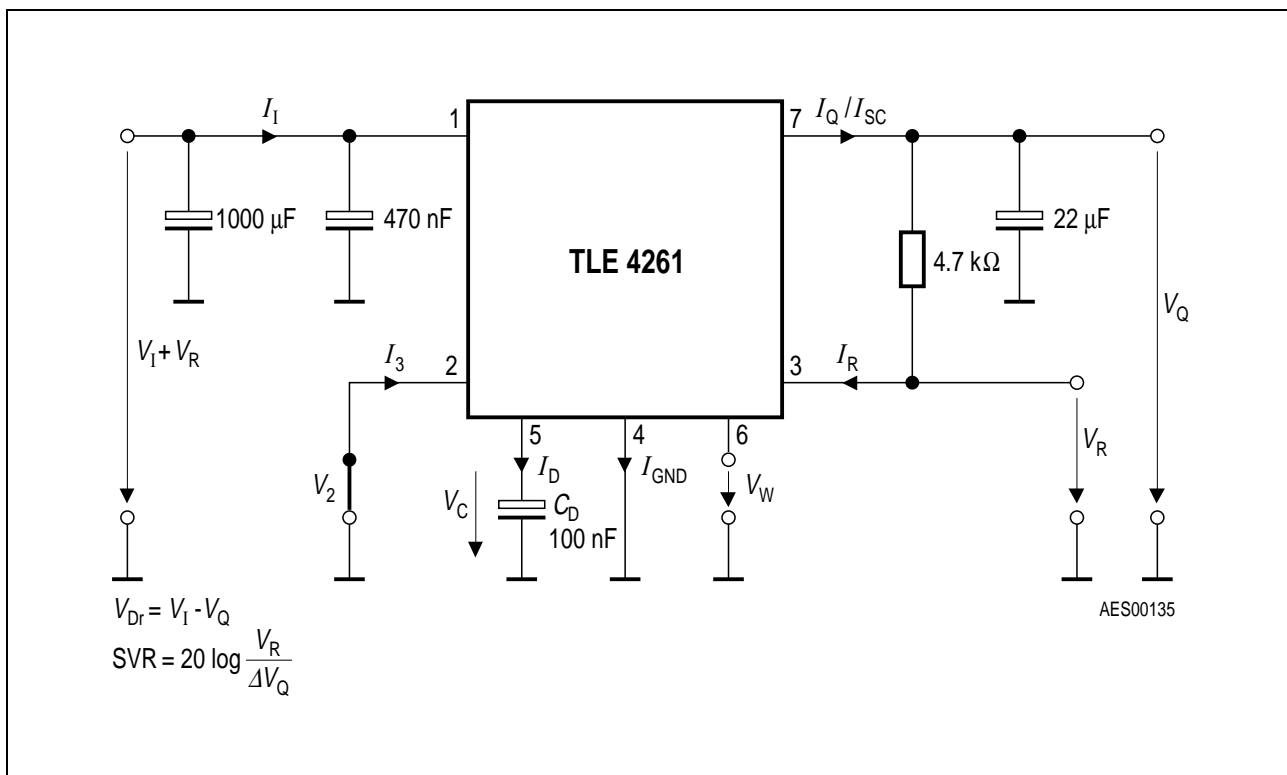
Turn-OFF voltage	V_W	5.2	5.6	6.0	V	–
Discharge current	I_{CD}	5.6	7.5	9.4	μA	$V_C = 1.5 \text{ V}$
Switching voltage	V_{CD}	2.95	3.05	3.15	V	–
Pulse interval	T_W	–	35	–	ms	$C_D = 100 \text{ nF}$

General Data

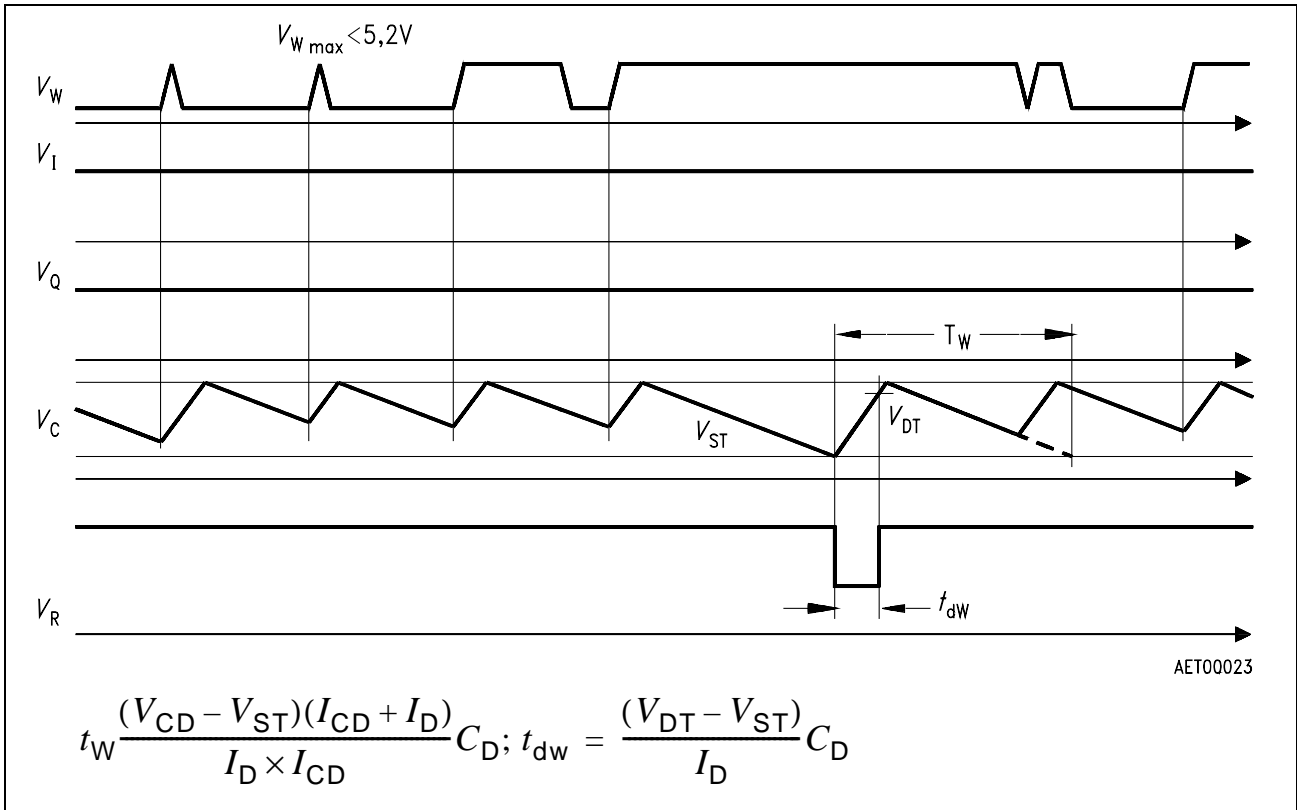
Turn-OFF voltage	V_{IOFF}	41	43	45	V	$I_Q < 1 \text{ mA}$
Turn-OFF hysteresis	ΔV_1	–	6.5	–	V	–
Leakage current	I_{QS}	–	–	50	μA	$V_Q = 0 \text{ V}$; $V_1 = 45 \text{ V}$
Reverse output current	I_{QR}	–	–	1.5	mA	$V_Q = 5 \text{ V}$; V_1 and V_2 open



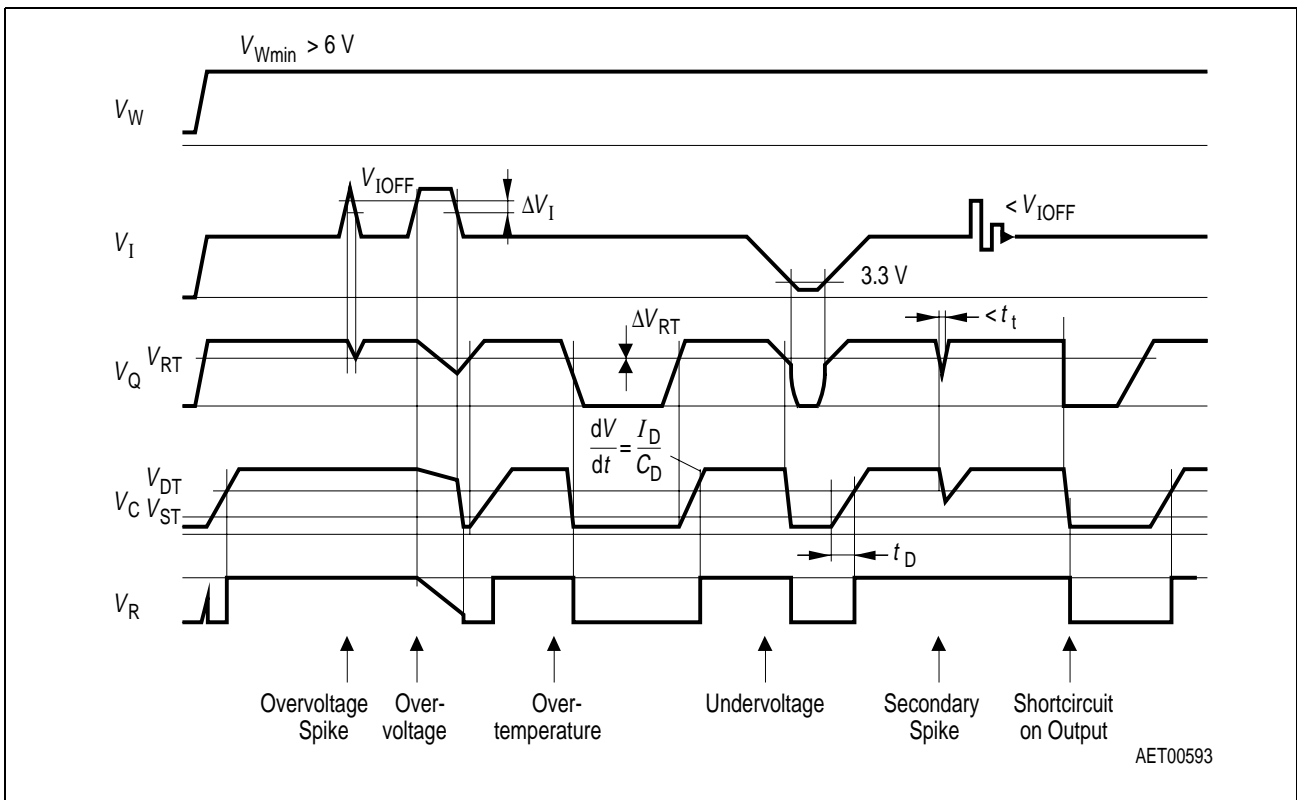
Application Circuit



Test Circuit

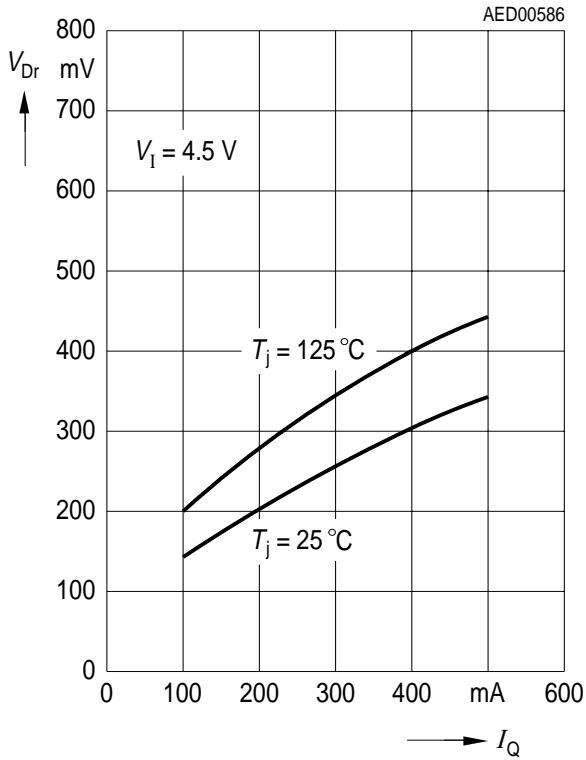


Time Response in Watchdog Condition

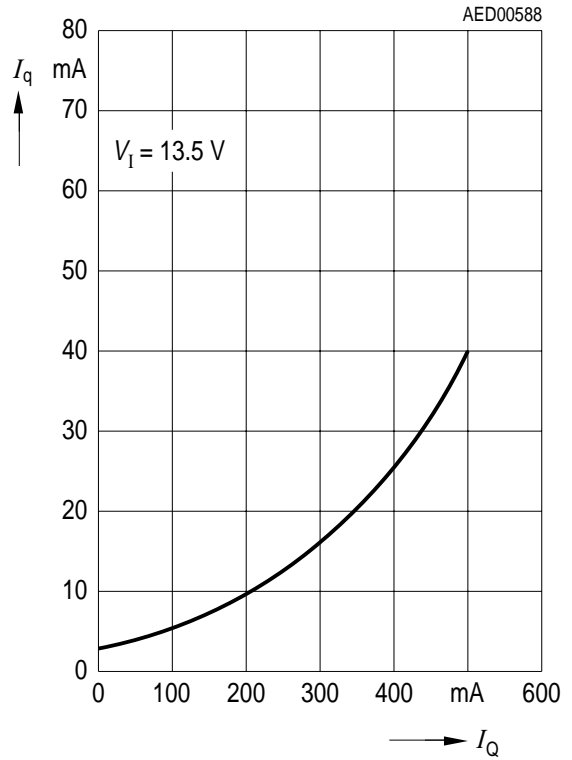


Timing with Watchdog OFF

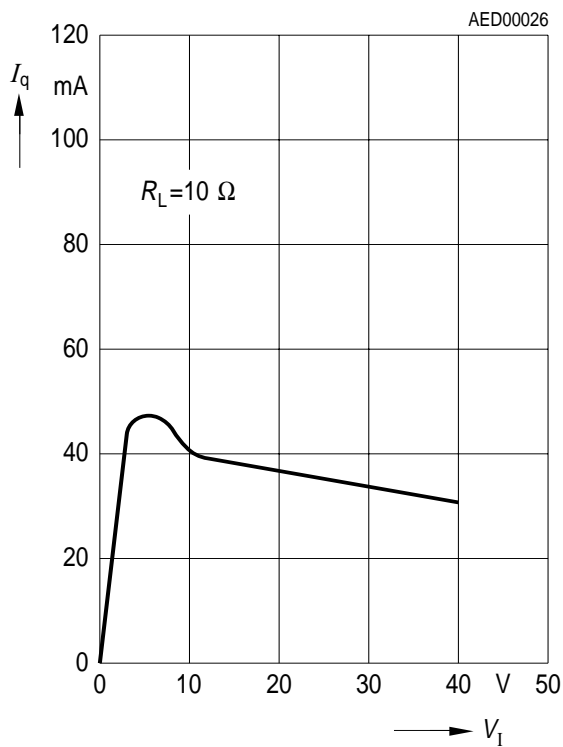
Drop Voltage versus Output Current



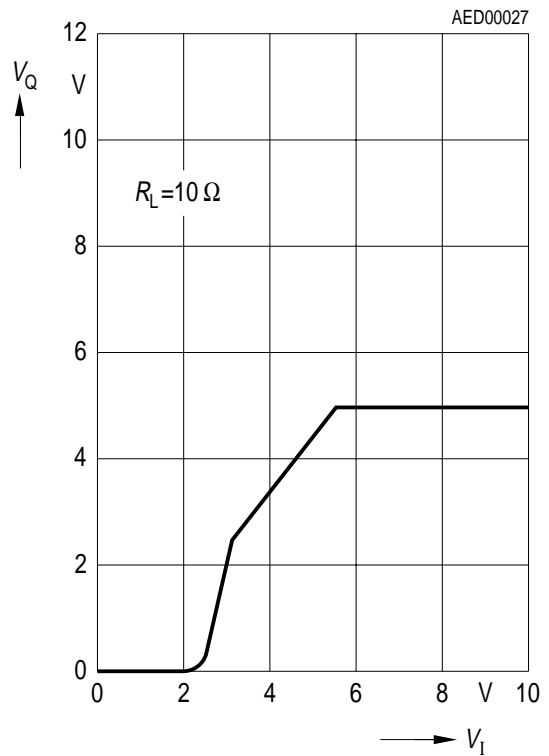
Current Consumption versus Output Current



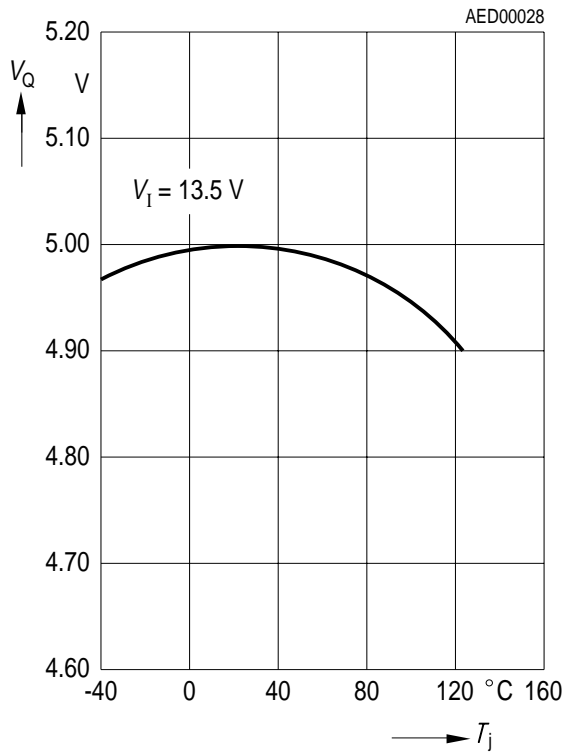
Current Consumption versus Input Voltage



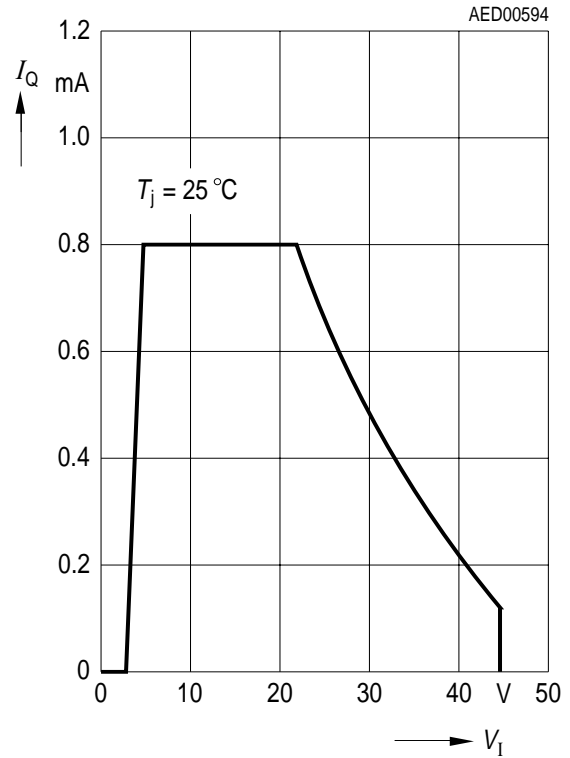
Output Voltage versus Input Voltage



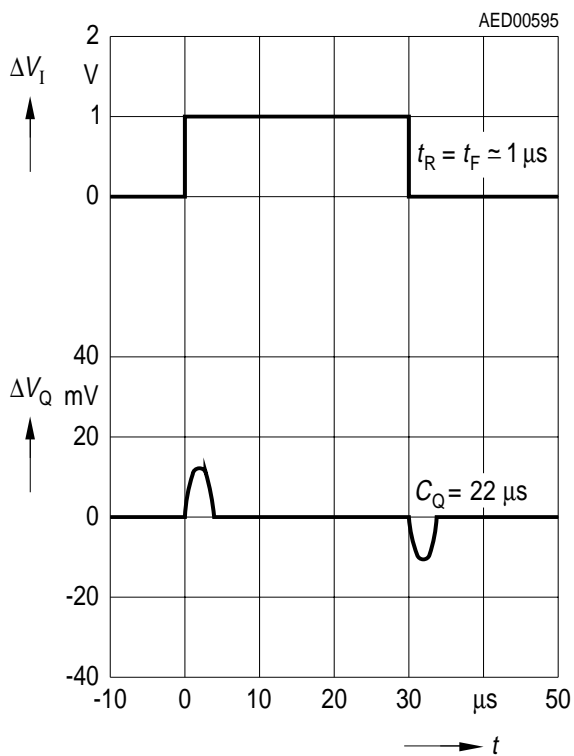
Output Voltage versus Temperature



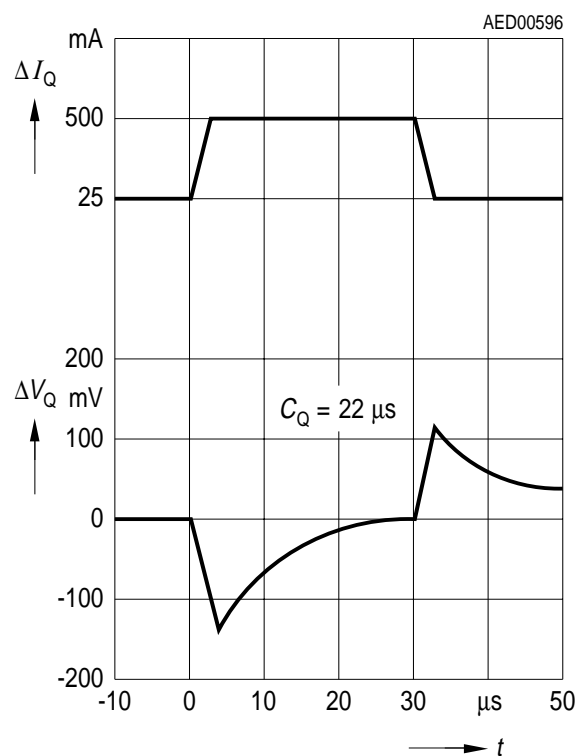
Output Current versus Input Voltage



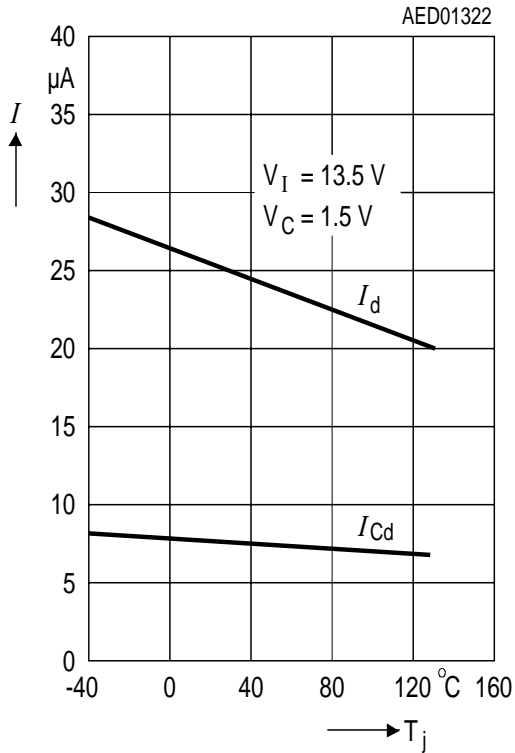
Input Step Response



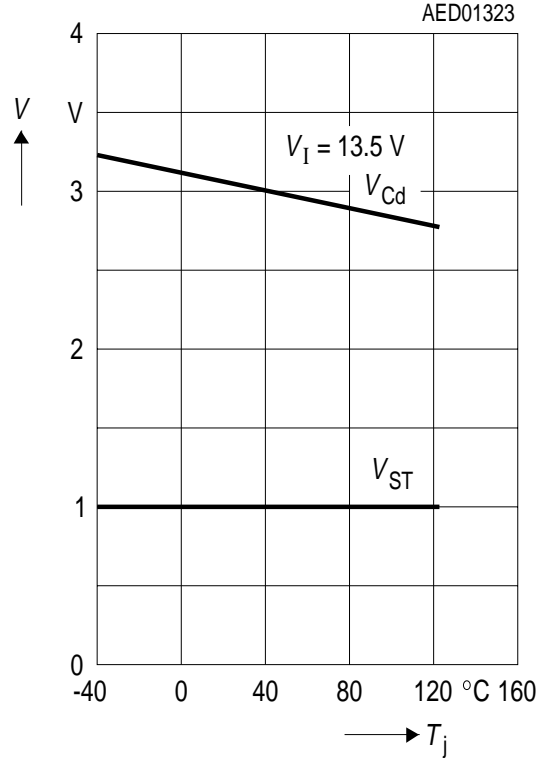
Load Step Response



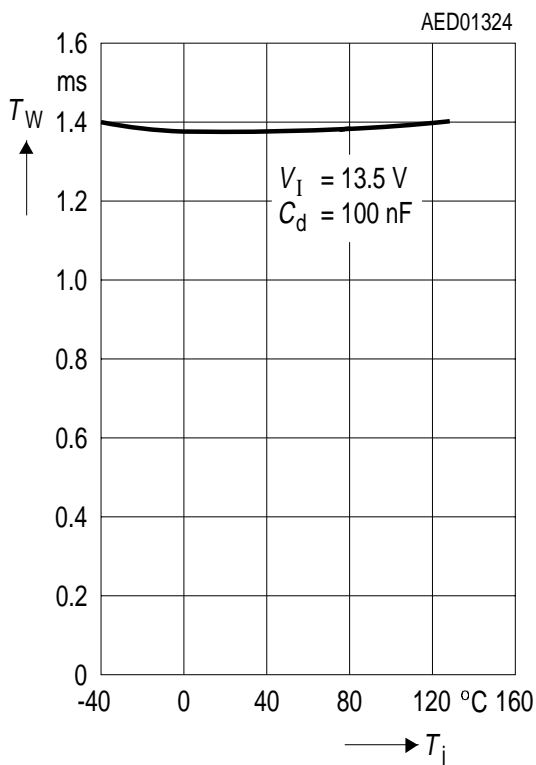
Charge Current I_D and Discharge Current I_{CD} versus Temperature



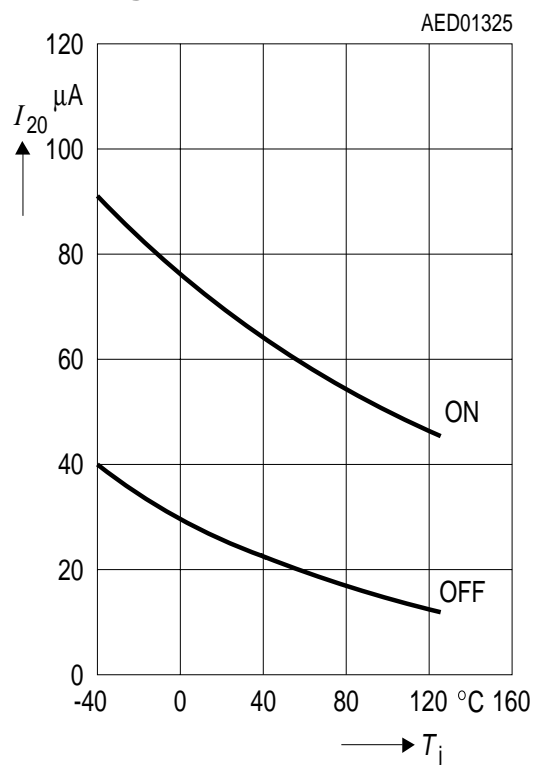
Switching Voltage V_{CD} and V_{ST} versus Temperature



Pulse Interval T_W versus Temperature



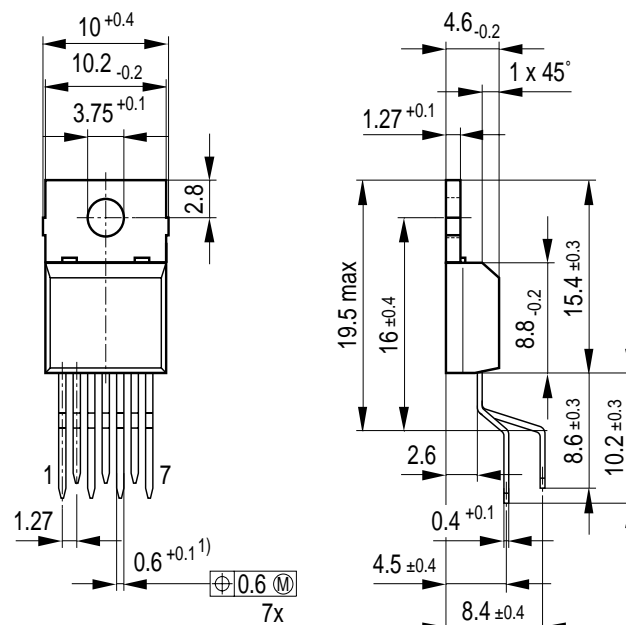
Current Consumption of Inhibit at the Switching Point versus Temperature



Package Outlines

P-TO220-7-1

(Plastic Transistor Single Outline)



1) $0.75_{-0.15}$ at dam bar (max 1.8 from body)

1) $0.75_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

GPT05108

Weight approx. 2.1 g

Sorts of Packing

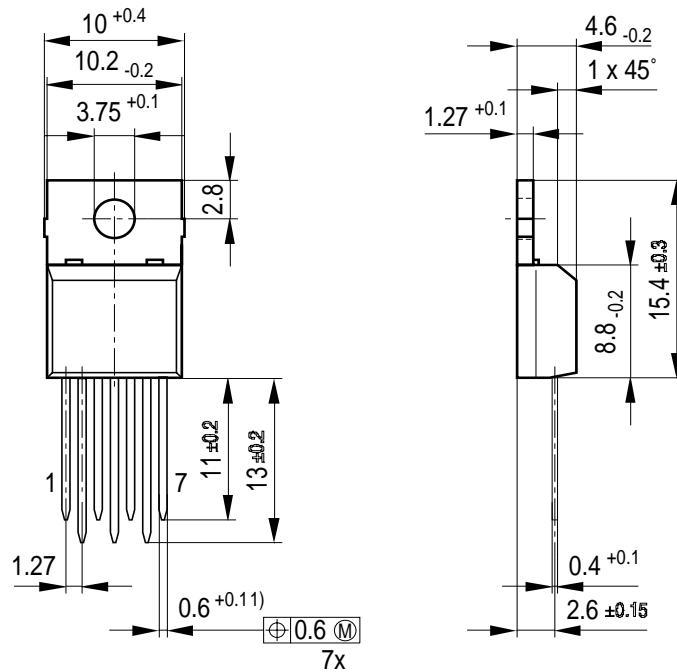
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

Package Outlines (cont'd)

P-TO220-7-2

(Plastic Transistor Single Outline)



- 1) $0.75_{-0.15}$ at dam bar (max 1.8 from body)
- 1) $0.75_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

Weight approx. 2.1 g

GPT05257

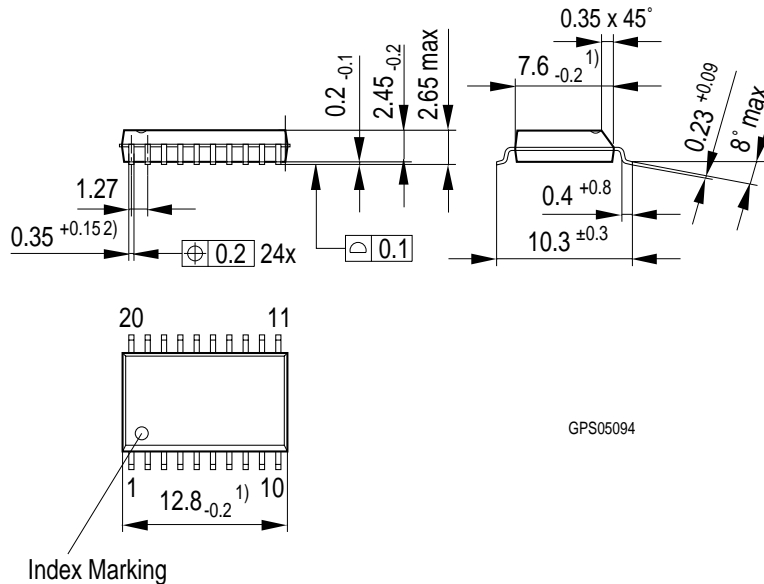
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

Package Outlines (cont'd)

P-DSO-20-6 (Plastic Dual Small Outline)



GPS05094

Index Marking

- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

Weight approx. 0.6 g

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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