NE/SE565
Phase-Locked Loop

Product Specification

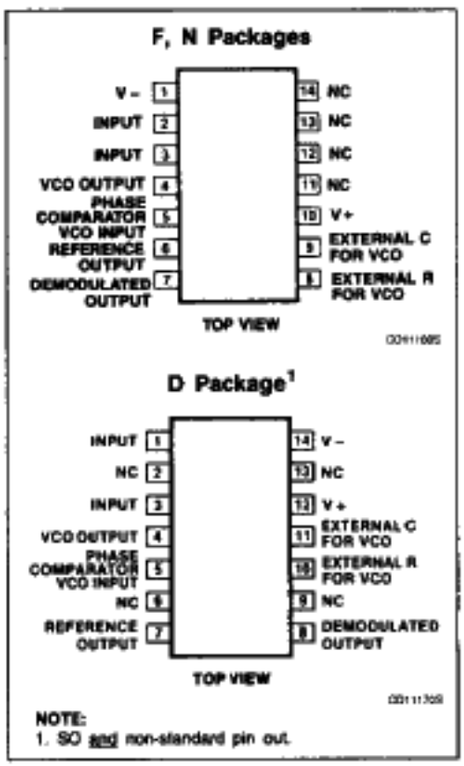
DESCRIPTION

The NE/SE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low pass filter as shown in the Block Diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (± 6V to ± 12V)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ± 1% to > ± 60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

PIN CONFIGURATIONS

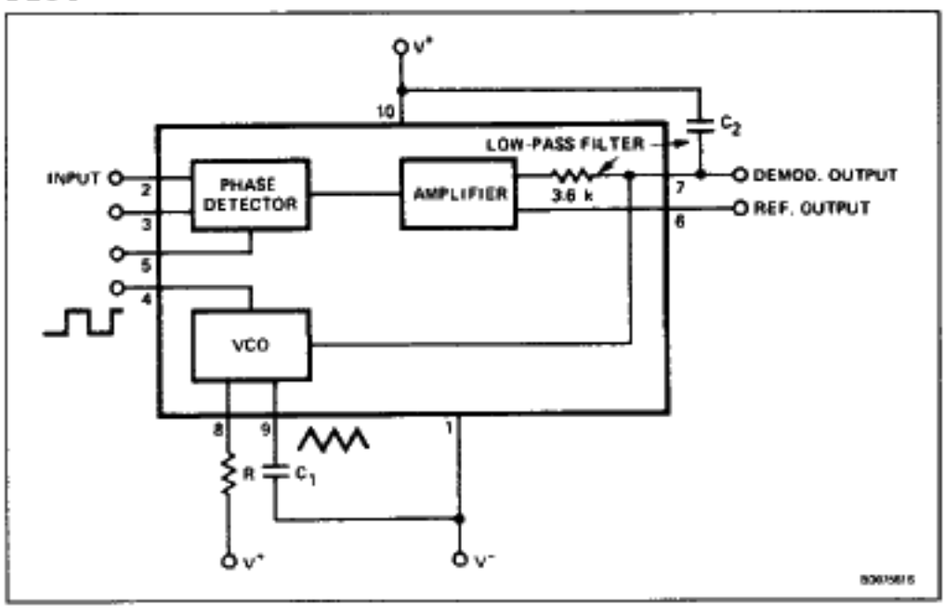


NOTE:
1. SO and non-standard pin out.

APPLICATIONS

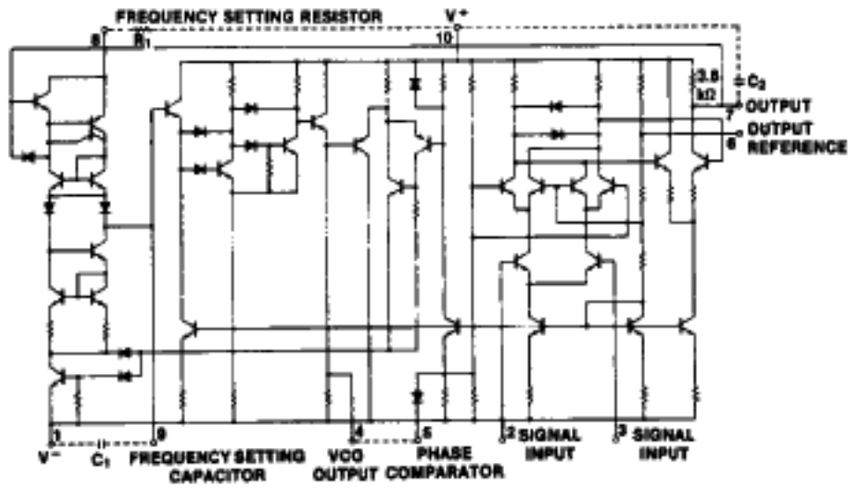
- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wide-band FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

BLOCK DIAGRAM



Phase-Locked Loop NE/SE565

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE565D
14-Pin Cerdip	0 to +70°C	NE565F
14-Pin Plastic DIP	0 to +70°C	NE565N
14-Pin Cerdip	−55°C to +125°C	SE565F
14-Pin Plastic DIP	−55°C to +125°C	SE565N

ABSOLUTE MAXIMUM RATINGS T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE565 SE565	 0 to +70 −55 to +125	 °C °C
P_D	Power dissipation	300	mW

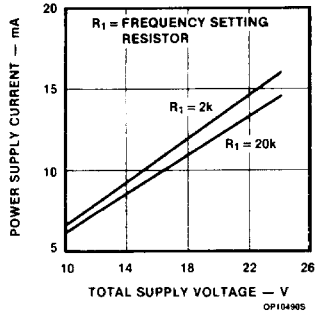
DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
			Min	Typ	Max	Min	Typ	Max	
Supply requirements									
V_{CC}	Supply voltage		±6		±12	±6		±12	V
I_{CC}	Supply current			8	12.5		8	12.5	mA
Input characteristics									
	Input impedance[1]		7	10		5	10		kΩ
	Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10			10			mV_{RMS}
VCO characteristics									
f_C	Center frequency Maximum value distribution[2]	Distribution taken about f_O = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	300 −10	500 0	 +10	 −30	500 0	 +30	kHz %
	Drift with temperature Drift with supply voltage	f_O = 50kHz f_O = 50kHz, V_{CC} = ±6 to ±7V		500 0.1	 1.0		600 0.2	 1.5	ppm/°C %/V
	Triangle wave output voltage level linearity		1.9	2.4 0.2	3	1.9	2.4 0.5	3	V_{P-P} %
	Square wave logical "1" output voltage logical "0" output voltage	 f_O = 50kHz f_O = 50kHz	 +4.9	 +5.2 −0.2	 +0.2	 +4.9	 +5.2 −0.2	 +0.2	 V V
	Duty cycle	f_O = 50kHz	45	50	55	40	50	60	%
t_R	Rise time			20	100		20		ns
t_F	Fall time			50	200		50		ns
I_{SINK}	Output current (sink)		0.6	1		0.6	1		mA
I_{SOURCE}	Output current (source)		5	10		5	10		mA
Demodulated output characteristics									
V_{OUT}	Output voltage level	Measured at Pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
	Maximum voltage swing[3]			2			2		V_{P-P}
	Output voltage swing	±10% frequency deviation	250	300		200	300		mV_{P-P}
THD	Total harmonic distortion			0.2	0.75		0.4	1.5	%
	Output impedance[4]			3.6			3.6		kΩ
V_{OS}	Offset voltage (V6 − V7)			30	100		50	200	mV
	Offset voltage vs temperature (drift)			50			100		μV/°C
	AM rejection		30	40			40		dB

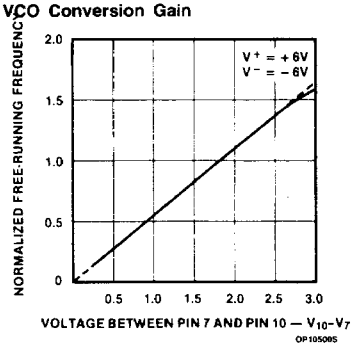
NOTES:
1. Both input terminals (Pins 2 and 3) must receive identical DC bias. This bias may range from 0V to −4V.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

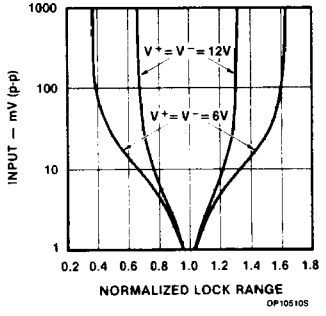
Power Supply Current as a Function of Supply Voltage



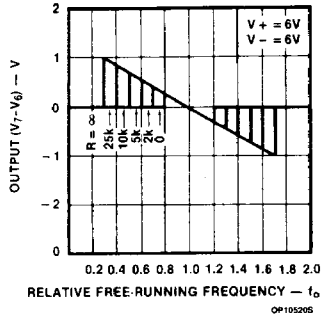
VCO Conversion Gain



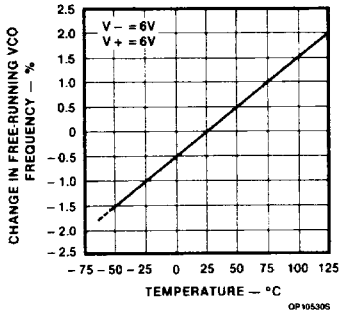
Lock Range as a Function of Input Voltage



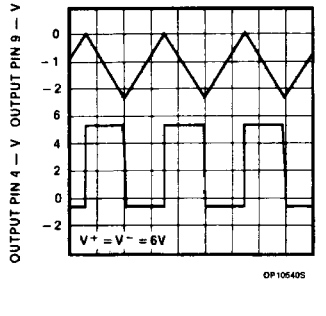
Lock Range as a Function of Gain Setting Resistance (Pins 6 - 7)



Change in Free-Running VCO Frequency as a Function of Temperature



VCO Output Waveform



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO:

$$f_O \simeq \frac{1.2}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase-Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average DC level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$$f_O \simeq \frac{1.2}{4R_1C_1}$$

and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000Ω with an optimum value on the order of 4000Ω. The source can be direct coupled if the DC resistances seen from Pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between Pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (Pin 7). Thus, if a resistance is connected between Pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_O to approximately ±20% of f_O (at ±6V).

A small capacitor (typically 0.001μF) should be connected between Pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between Pin 7 and the positive supply, and an internal resistance of approximately 3600Ω.

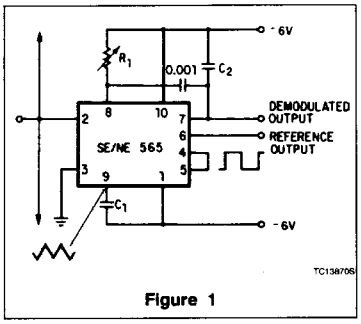


Figure 1

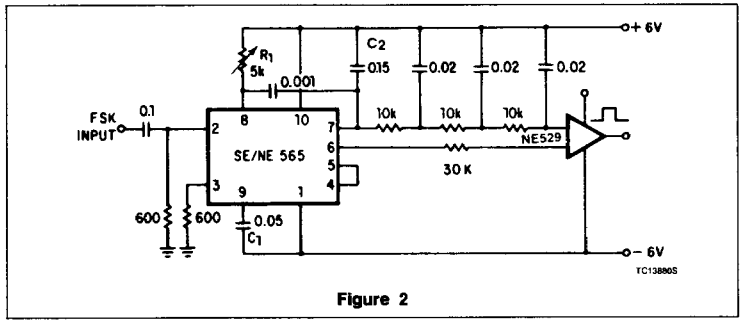


Figure 2

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" to "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding DC shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and Pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

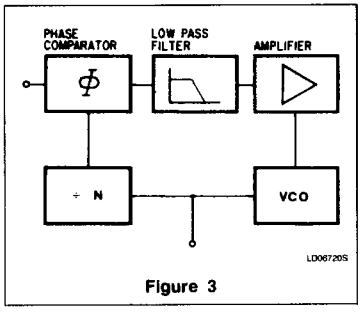


Figure 3

The input connection is typical for cases where a DC voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect at 600Ω input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at Pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

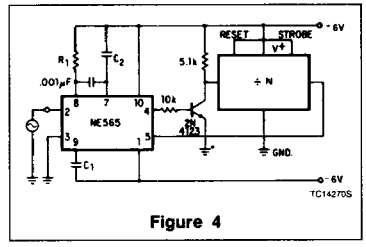


Figure 4

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this, a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase-Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (Pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000Ω.

The Phase-Locked Loop is tuned to 67kHz with a 5000Ω potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (Pin 7) passes through a three-stage low pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at Pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

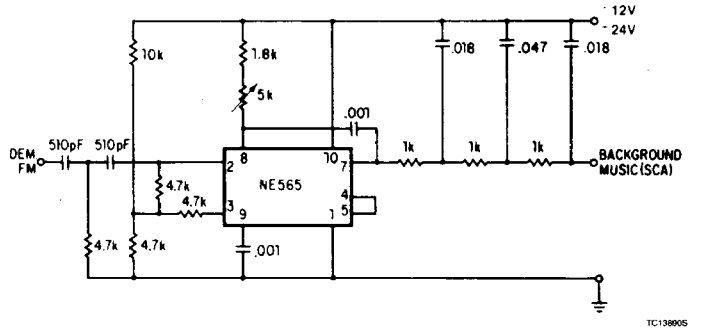


Figure 5