

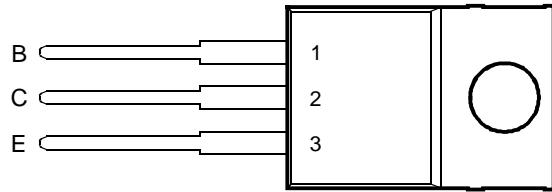
BD646, BD648, BD650, BD652 PNP SILICON POWER DARLINGTONS

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MAY 1993 - REVISED MARCH 1997

- **Designed for Complementary Use with BD645, BD647, BD649 and BD651**
- **62.5 W at 25°C Case Temperature**
- **8 A Continuous Collector Current**
- **Minimum h_{FE} of 750 at 3 V, 3 A**

**TO-220 PACKAGE
(TOP VIEW)**



Pin 2 is in electrical contact with the mounting base.

MDTRACA

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Collector-base voltage ($I_E = 0$)	BD646	V_{CBO}	-80	V
	BD648		-100	
	BD650		-120	
	BD652		-140	
Collector-emitter voltage ($I_B = 0$)	BD646	V_{CEO}	-60	V
	BD648		-80	
	BD650		-100	
	BD652		-120	
Emitter-base voltage		V_{EBO}	-5	V
Continuous collector current		I_C	-8	A
Peak collector current (see Note 1)		I_{CM}	-12	A
Continuous base current		I_B	-0.3	A
Continuous device dissipation at (or below) 25°C case temperature (see Note 2)		P_{tot}	62.5	W
Continuous device dissipation at (or below) 25°C free air temperature (see Note 3)		P_{tot}	2	W
Unclamped inductive load energy (see Note 4)		$\frac{1}{2}LI_C^2$	50	mJ
Operating junction temperature range		T_j	-65 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C
Lead temperature 3.2 mm from case for 10 seconds		T_L	260	°C

- NOTES: 1. This value applies for $t_p \leq 0.3$ ms, duty cycle $\leq 10\%$.
 2. Derate linearly to 150°C case temperature at the rate of 0.4 W/°C.
 3. Derate linearly to 150°C free air temperature at the rate of 16 mW/°C.
 4. This rating is based on the capability of the transistor to operate safely in a circuit of: $L = 20$ mH, $I_{B(on)} = -5$ mA, $R_{BE} = 100 \Omega$, $V_{BE(off)} = 0$, $R_S = 0.1 \Omega$, $V_{CC} = -20$ V.

PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.



BD646, BD648, BD650, BD652

PNP SILICON POWER DARLINGTONS

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electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)CEO}$ Collector-emitter breakdown voltage	$I_C = -30 \text{ mA}$	$I_B = 0$ (see Note 5)	BD646 BD648 BD650 BD652	-60 -80 -100 -120		V
I_{CEO} Collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$ $V_{CE} = -40 \text{ V}$ $V_{CE} = -50 \text{ V}$ $V_{CE} = -60 \text{ V}$	$I_B = 0$	BD646 BD648 BD650 BD652		-0.5 -0.5 -0.5 -0.5	mA
I_{CBO} Collector cut-off current	$V_{CB} = -60 \text{ V}$ $V_{CB} = -80 \text{ V}$ $V_{CB} = -100 \text{ V}$ $V_{CB} = -120 \text{ V}$ $V_{CB} = -40 \text{ V}$ $V_{CB} = -50 \text{ V}$ $V_{CB} = -60 \text{ V}$ $V_{CB} = -70 \text{ V}$	$I_E = 0$	BD646 BD648 BD650 BD652	$T_C = 150^\circ\text{C}$ $T_C = 150^\circ\text{C}$ $T_C = 150^\circ\text{C}$ $T_C = 150^\circ\text{C}$	-0.2 -0.2 -0.2 -0.2 -2.0 -2.0 -2.0 -2.0	mA
I_{EBO} Emitter cut-off current	$V_{EB} = -5 \text{ V}$	$I_C = 0$ (see Notes 5 and 6)			-5	mA
h_{FE} Forward current transfer ratio	$V_{CE} = -3 \text{ V}$	$I_C = -3 \text{ A}$ (see Notes 5 and 6)		750		
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_B = -12 \text{ mA}$ $I_B = -50 \text{ mA}$	$I_C = -3 \text{ A}$ $I_C = -5 \text{ A}$ (see Notes 5 and 6)			-2 -2.5	V
$V_{BE(sat)}$ Base-emitter saturation voltage	$I_B = -50 \text{ mA}$	$I_C = -5 \text{ A}$ (see Notes 5 and 6)			-3	V
$V_{BE(on)}$ Base-emitter voltage	$V_{CE} = -3 \text{ V}$	$I_C = -3 \text{ A}$ (see Notes 5 and 6)			-2.5	V

NOTES: 5. These parameters must be measured using pulse techniques, $t_p = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

6. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts.

thermal characteristics

PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JC}$ Junction to case thermal resistance			2.0	$^\circ\text{C/W}$
$R_{\theta JA}$ Junction to free air thermal resistance			62.5	$^\circ\text{C/W}$

TYPICAL CHARACTERISTICS

TYPICAL DC CURRENT GAIN
VS
COLLECTOR CURRENT

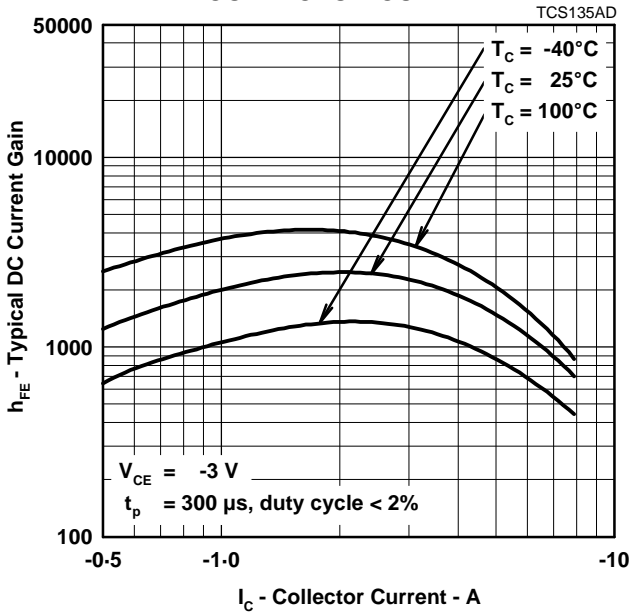


Figure 1.

COLLECTOR-EMITTER SATURATION VOLTAGE
VS
COLLECTOR CURRENT

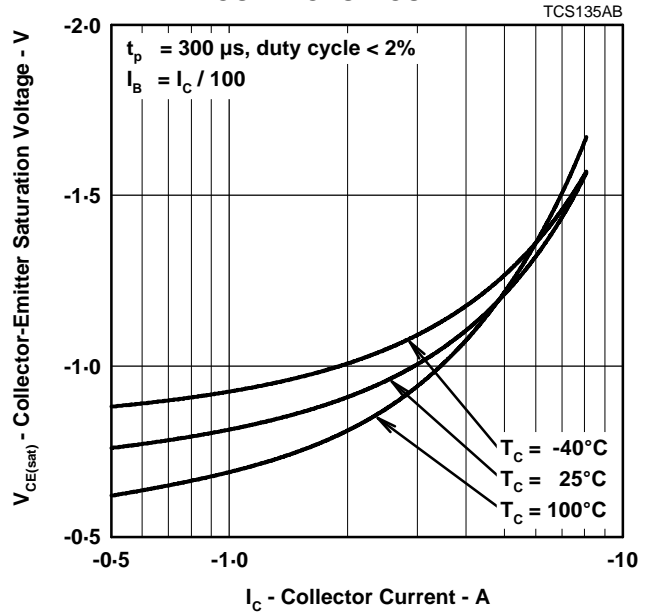


Figure 2.

BASE-EMITTER SATURATION VOLTAGE
VS
COLLECTOR CURRENT

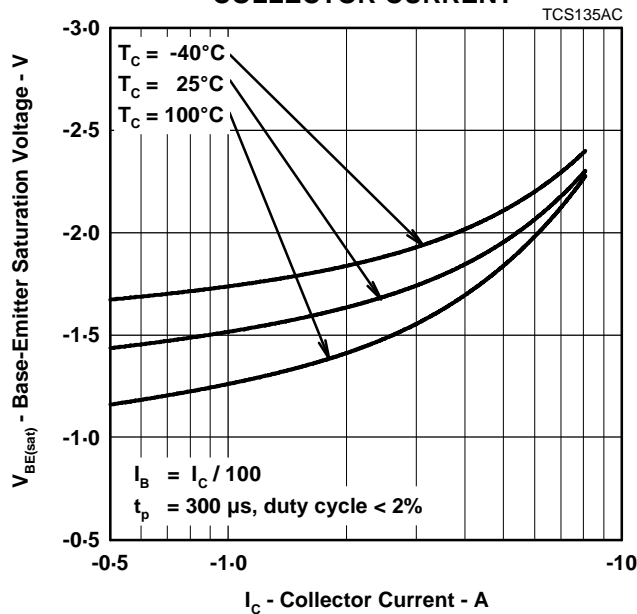


Figure 3.

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MAXIMUM SAFE OPERATING REGIONS

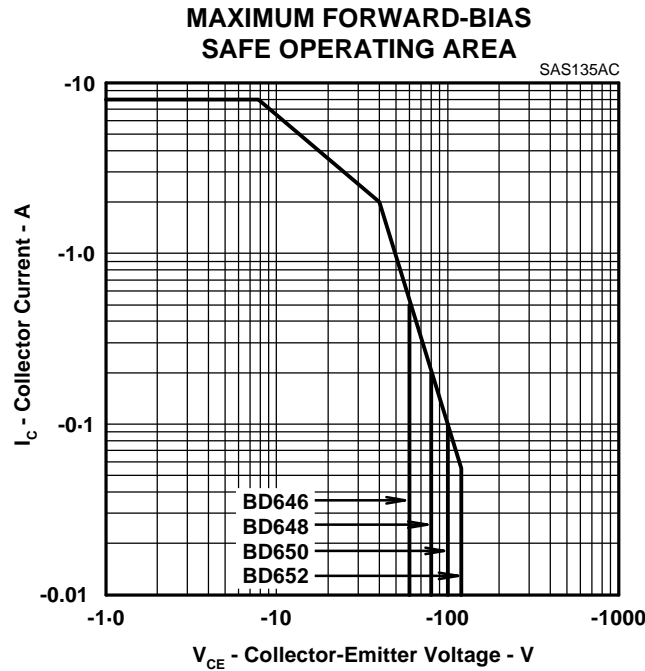


Figure 4.

THERMAL INFORMATION

MAXIMUM POWER DISSIPATION VS CASE TEMPERATURE

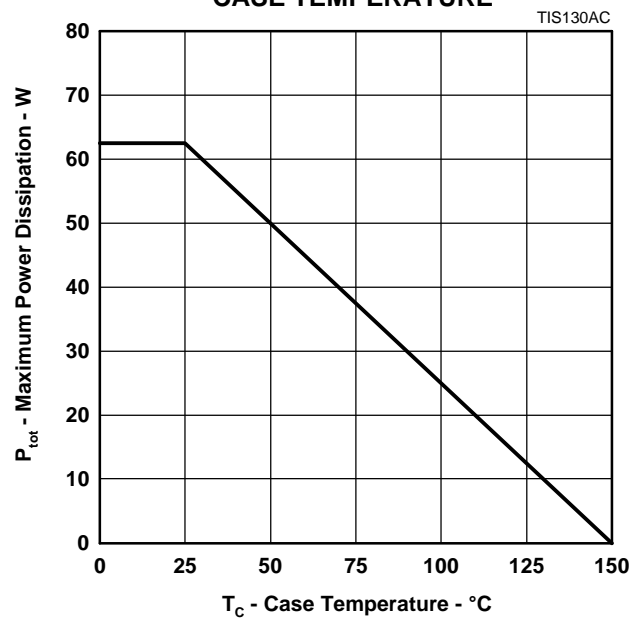


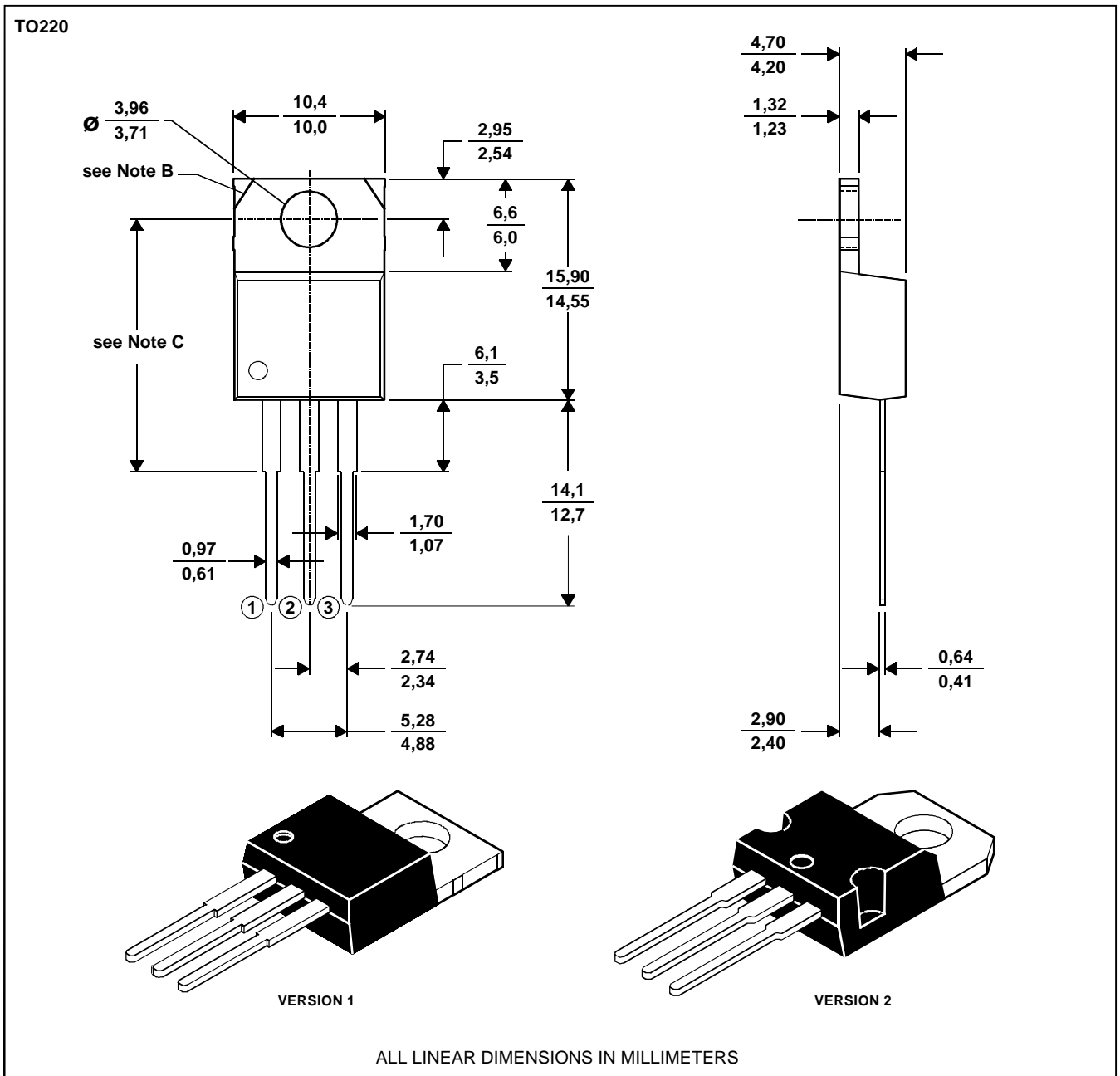
Figure 5.

MECHANICAL DATA

TO-220

3-pin plastic flange-mount package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. The centre pin is in electrical contact with the mounting tab.
 B. Mounting tab corner profile according to package version.
 C. Typical fixing hole centre stand off height according to package version.
 Version 1, 18.0 mm. Version 2, 17.6 mm.

MDXXBE

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PRODUCT INFORMATION