PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

TMP82C79P-2/TMP82C79M-2

1. GENERAL DESCRIPTION

The TMP82C79P-2/M-2 (hereinafter referred to as TMP82C79) is a programmable keyboard/display interface. The keyboard portion can provide a scanned interface up to 64-contact key matrix. Also, the keyboard portion can interface to an array of sensors or a strobed interface keyboard. Key depressions can be 2-key lockout or N-key rollover. The display portion has 16×8 bits display RAM which can be treated as dual 16×4 bits. Both right entry and left entry display formats are possible.

2. FEATURES

- Simultaneous Keyboard Display operation.
- Scanned Keyboard mode.
- Scanned Sensor matrix mode.
- Strobed Input Entry mode.
- Built-in 8-Character FIFO or 64 bit Sensor RAM.
- Programmable 2-key Lockout or N-key Rollover with contact debounce.
- Built-in 16×8bit Display RAM
- Programmable scan timing.
- Extend operating temperature range −40 °C to +85 °C.

3. PIN CONNECTION

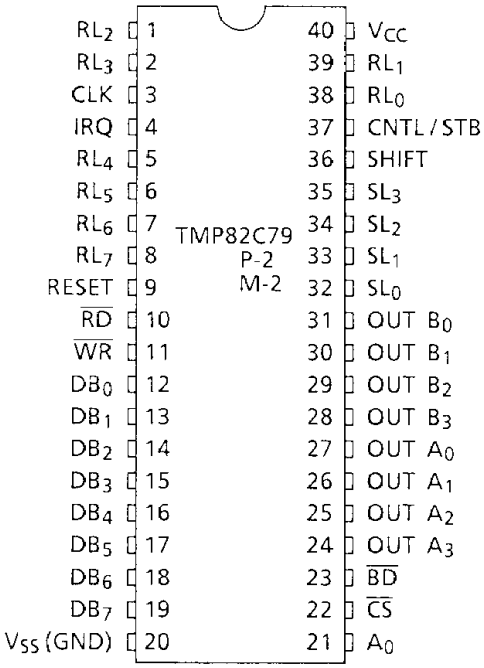

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Figure 3.1 Pin Connection

4. BLOCK DIAGRAM

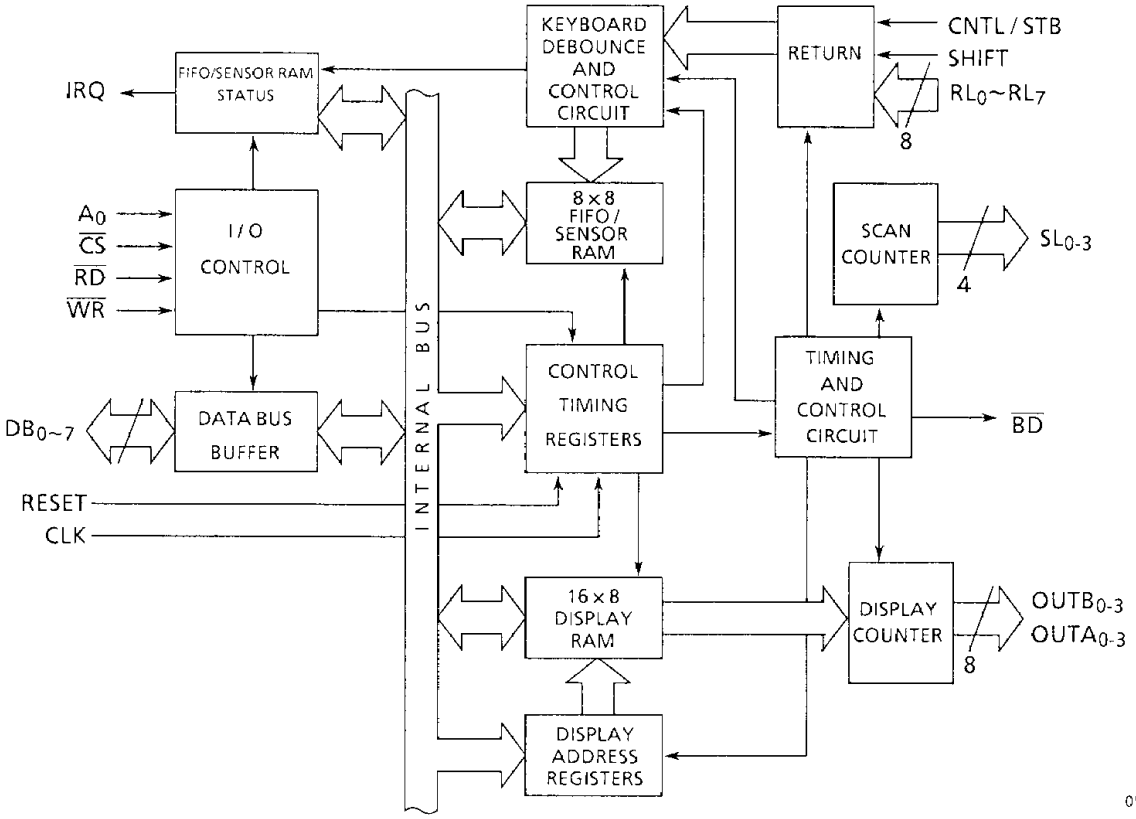

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Figure 4.1 Block Diagram

5. PIN NAMES AND PIN DESCRIPTION

- VSS (Power Supply)

  Gound

- VCC (Power Supply)

  +5V during operation

- DB_0-DB_7 (Input/Output)

  Bidirectional data bus. All data and commands are transferred via this data bus.

- CLK (Input)

  System Clock used to generate the TMP82C79 internal timing.

- RESET (Input)

  A high level signal on this pin resets the TMP82C79. After being reset the TMP82C79 is placed in the following state.

  (1)16×8 bit character display, left entry.

  (2)Encode scan keyboard, 2 key lockout, clock pre-scale value is set to 31.

- $\overline{CS}$ (Input)

  A low level input on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the MPU and the TMP82C79.

- A_0 (Input)

  This input acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. A high level on this pin indicates the signals on data bus are interpreted as command or status. A low level indicates they are data in the RAMs.

- $\overline{WR}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP82C79 to accept command or data from the MPU.

- $\overline{RD}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP82C79 to output data or status onto the data bus.

- IRQ (Output)

  Interrupt request output. In keyboard mode, the interrupt line is high when the FIFO/Sensor RAM has effective data. The interrupt line goes low when each FIFO/Sensor RAM is read and returns high if the RAM still has effective data. In sensor matrix mode, the interrupt line goes high whenever any change in the sensor matrix is detected.

- SL_0-SL_3 (Output)

  Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).

- RL_0-RL_7 (Input)

  Return lines which are connected to the scan lines through the key or sensor switches. Each line has an internal pullup to keep it high until a switch closure pulls it low. They also serve as an 8-bit input in Strobed Input mode.

- SHIFT (Input)

  This input status is stored in the FIFO RAM in addition to the information of the key position on key closure in Scanned key board modes. It has an internal pullup to keep it high until a switch closure pulls it low.

- CNTL/STB (Input)

  For Keyboard modes this line is used as a control input and stored like status on a key closure. This can be also programmed as the strobe line that enters the data into FIFO in Strobed Input mode (Rising Edge). It has an internal pullup to keep it high until a switch closure pulls it low.

  $OUTA_0$-$OUTA_3$ (Output)

  $OUTB_0$-$OUTB_3$ (Output)

  These two ports are the outputs for the 16×4 display refresh registers. The data from these outputs is updated synchronized with the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be treated as one 8-bit port.

- $\overline{BD}$ (Output)

  This output is used to blank the display during digit switching or by a display blanking command.

6. FUNCTIONAL DESCRIPTION

6.1 I/O CONTROL AND DATA BUS BUFFER

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines and controls the flow of data to and from the various internal registers and buffers in the TMP82C79. $\overline{CS}$ input enables the all data flow to and from the TMP82C79. The character of the information given by the MPU, is identified by A_0.

$\overline{RD}$ and $\overline{WR}$ decide the direction of data flow through the data bus buffer. The data bus buffer is bidirectional buffer which is used for connecting the internal bus and a system bus. When $\overline{CS}$ is high, the buffer is in a high impedance state.

6.2 CONTROL REGISTER, TIMING REGISTER AND TIMING CONTROL CIRCUIT

Keyboard and display modes and the other operating conditions are programmed by the MPU. These modes are latched at the rising edge of $\overline{WR}$ when A_0 is high. The timing control contains the basic counter chains. The first counter is the 1/N prescaler that can be programmed to yield an basic internal frequncy. In case of 100kHz basic internal frequency, it gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan and display scan timings.

6.3 SCAN COUNTER

Two modes are available for the scan counter. In the encode mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the key board and display. In the decode mode, the scan counter decodes the least significant 2 bits internally and provides a decoded 1 of 4 scan. Note that the only first 4 characters in the Display RAM are outputted from $OUTA_{0-3}$ and $OUTB_{0-3}$ in the decode mode.

6.4 RETURN BUFFER AND KEYBOARD DEVOUNCE CONTROL CIRCUIT

The 8 return lines are latched onto the return line buffer. In the Keyboard mode, these lines are scanned to look for key closures in a row. If the debounce circuit detects a closed switch, it waits about *10 ms, and checks if the switch remains closed. If it does so, the address of the switch and the status of SHIFT and CNTL lines is transferred to the FIFO.

In the scanned Sensor Matrix Modes, the contents of the return lines are directly transferred to the corresponding row of the sensor RAM (FIFO) each scan time.

In the Strobed Input Mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

6.5 FIFO/SENSOR RAM AND FIFO/SENSER RAM STATUS

The FIFO/Sensor RAM is a dual function RAM. In the keyboard mode or In the Strobe Input mode, this RAM serves as a FIFO. The FIFO status shows whether the FIFO is empty or full and keeps the number of characters in the FIFO. In addition, there is a flag to show an error in the case where too many reads or writes is recognized. The FIFO status can be read at $\overline{CS}=\overline{RD}=0$, $A_0=1$. The FIFO status logic provides an IRQ signal when the FIFO is not empty. In the scanned sensor matrix mode, the RAM serves as a sensor RAM. IRQ becomes high when a change in the sensor is detected.

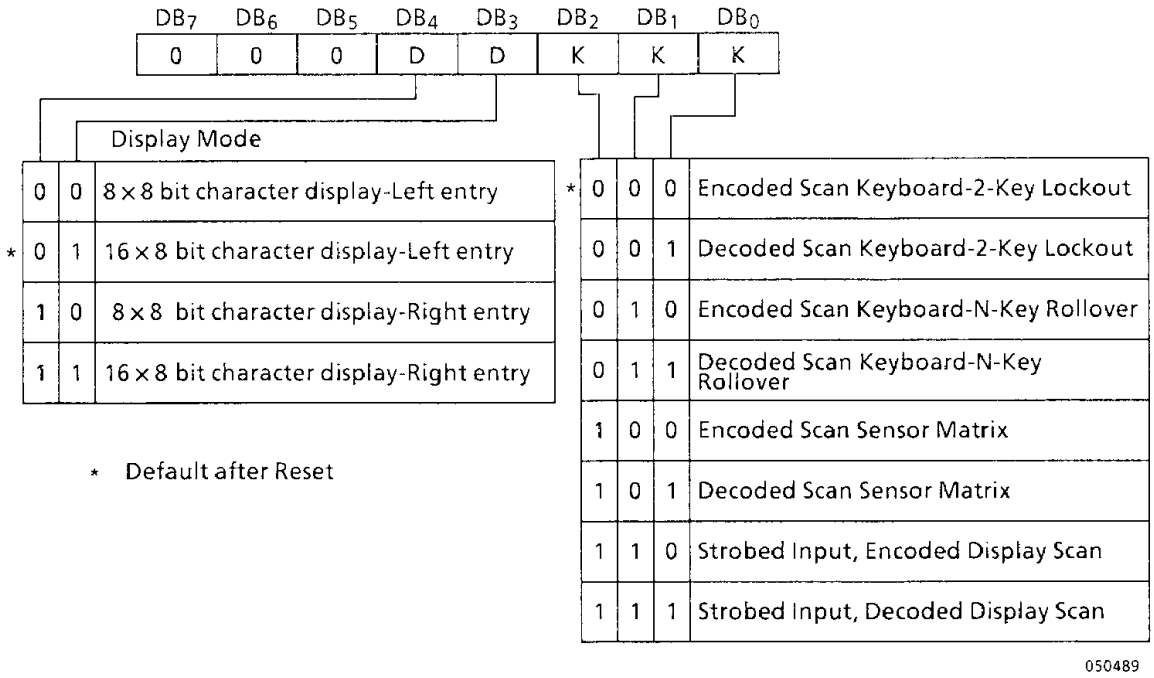
6.6 DISPLAY ADDRESS REGISTERS AND DISPLAY RAM

The display address registers hold the address of the word currently being written or read by the MPU and the two 4 bit nibbles being displayed. The Display RAM stores data for display outputs. The read/write addresses are programmed by the MPU command. They also can be programmed to autoincrement after read or write. The Display RAM can be directry read out by the MPU after mode and address is set. The A and B nibbles of the Display RAM are outputted to the Display Output A and B synchronously with scan signals (SL_0-SL_3). The A and B nibbles can be entered independently or as one word by the MPU command.

* In case of 100kHz basic internal frequency

7. COMMAND DESCRIPTION

7.1 KEYBOARD/DISPLAY MODE SET



* Default after Reset

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7.2 PROGRAM CLOCK

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	P	P	P	P	P

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The TMP82C79 generates all timing and multiplexing signals by means of the internal prescaler. The prescaler generates internal reference clocks by dividing an external supply clock by a programmable value PPPPP. Any number from 2 to 31 can be set as a prescaler value. When this value is set to 0 or 1, it is interpreted to be 2. If the internal reference clock is set to 100kHz, it is possible to obtain 5.1ms keyboard scan time and 10.3ms debounce time. The value PPPPP is set to 31 after reset, but cannot be changed by the Clear command.

7.3 READ FIFO/SENSOR RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	0	AI	×	A	A	A

× = don't care 050489

If this command is written, the subsequent data reads are set up for the FIFO/Sensor RAM. Auto-increment flag (AI) and the RAM address bits AAA are valid only in Senser Matrix Mode. The address bits AAA select one of the 8 rows of the Sensor RAM. If AI = 1, the RAM address is incremented after each successive read. The Auto-increment flag does not affect the auto-increment of the Display RAM.

7.4 READ DISPLAY RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	1	AI	A	A	A	A

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If this command is written, the subsequent data reads are set up for the Display RAM. The address bits AAAA select one of the 16 rows of the Display RAM. If AI = 1, the address is incremented after each read or write to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read or wirte address and the sense of the Auto-increment for both operation.

7.5 WRITE DISPLAY RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	AI	A	A	A	A

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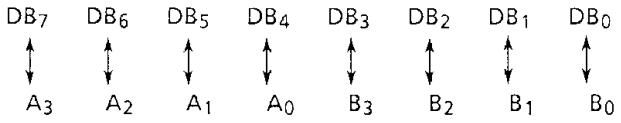
If this command is written, the subsequent data writes are set up for the Display RAM. Note that writing this command does not switch the source of the subsequent data reads. The address register of the Display RAM is same for read/write operations. The addressing and Auto-increment function are identical to those for the Read Display RAM.

7.6 DISPLAY WRITE INHIBIT/BLANKING

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	1	×	IWA	IWB	BLA	BLB

× = don't care 050489

The IWA or IWB bit can be used to mask A nibble or B nibble for entering the Display data independently. The BLA of BLB flag is available for the nibble A or B to blank the display. In the case where the Display Outputs are used as separate 4-bit display ports, the IWA or IWB bit is useful so as not to affect the other display port when the MPU writes a word to the display RAM. The BLA or BLB bit is used for blanking the display independently without giving any affect to the other 4-bit display port. The blank code is determined by the last Clear command that has been programmed after reset. If the Display Output is used as an 8-bit port, it is necessary to set both BLA and BLB bits for blnaking the display. Then $\overline{BD}$ signal becomes low.



Correspondence between Display Output and Data Bus

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7.7 CLEAR

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	CD	CD	CD	CF	CA

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The CD bits are used to clear all rows of the Display RAM to the following code shown below.

(DB4) CD	(DB3) CD	(DB2) CD	
1	0	×	···· All Zeros (X = Don't Care)
1	1	0	···· All Hex 20H (0010 0000)
1	1	1	···· All Ones
0	×	×	···· not clear display if CA = 0
↑			Enable clear display when CD = 1 (or by CA = 1)

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While the Display RAM is being cleared, it may not write to the Display RAM. The MSB bit of the FIFO status word is set during this time. If the CF bit is set to "1", the FIFO status is cleared and the interrupt request output (IRQ) is reset. Also, the Senser RAM pointer is set to the row 0.

The CA bit has the combined effect of the CD bit and CF bit. It enables clear display code to the Display RAM and also clears the FIFO status. Furthermore, it re-synchronizes the internal timing chains.

7.8 END INTERRUPT/ERROR MODE SET

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	E	×	×	×	×

× = don't care

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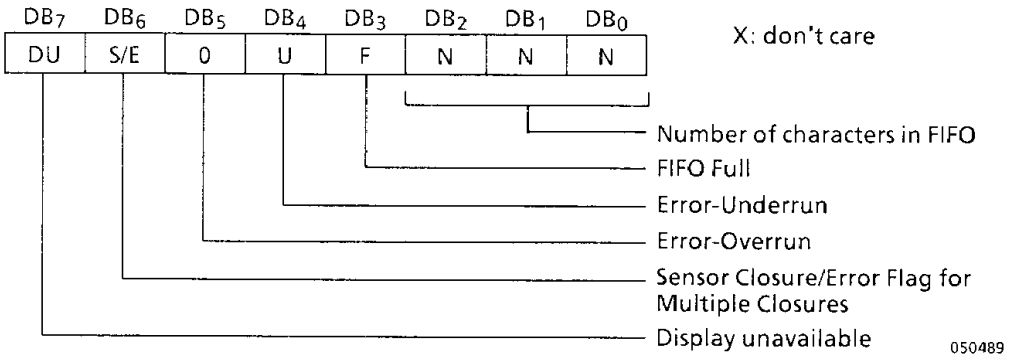
In the Sensor Matrix mode, this command loweres the IRQ line and enables writing to the sensor RAM. This means that a write to the Sensor RAM is inhibited when IRQ line is high. If the E bit is set to "1", the S/E bit of the FIFO status becomes "1" when any one of the sensor switches is closed. If E = 0, the S/E bit is always "0". In the N-Key Rollover mode, if the E bit is programmed to "1", the Special Error mode will be resulted.

7.9 FIFO STATUS



Du : Indicates that the Display RAM was unavailable because a Clear Display or Clear All command has not completed its clearing operation.

S/E : In a Sensor Matrix mode, if the E bit of End Interrupt/error mode set is programmed to "0", this S/E bit is set to indicate that at least one sensor closure indication is contained in the Sensor RAM.
In Special Error Mode, this S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.

O : indicates that the entry of another character into a full FIFO was attempted.

U : indicates that the MPU tried to read an empty FIFO.

F : indicates that the FIFO is full of the eight characters.

NNN : indicates number of characters in the FIFO when in the Keyboard Mode or in the Strobe Input Mode.

Table 7.1 ADDRESSING

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Functions
0	0	0	1	Read Data
0	0	1	0	Write Data
0	1	0	1	Read Status word
0	1	1	0	Write Command word
1	×	×	×	High-impedance state

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8. INTERFACE WITH KEYBOARD

8.1 SCANNED KEYBOARD, 2-KEY LOCKOUT

In this mode, if one key only is kept depressed during one debounce cycle (2 times of the key scan cycle), the key is recognized. When a key is depressed, the debounce logic is set and the other depressed keys are checked during the next two scan cycle. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If another depressed key are encountered, operates as follows.

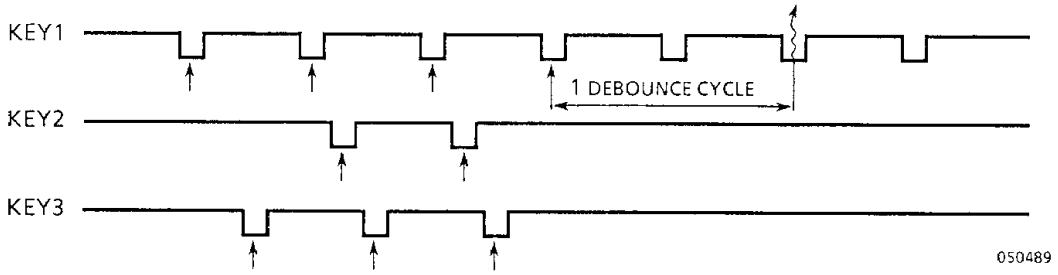

Figure 8.1 Example of a Case Where a First Depressed Key is Continuously Kept to the Last

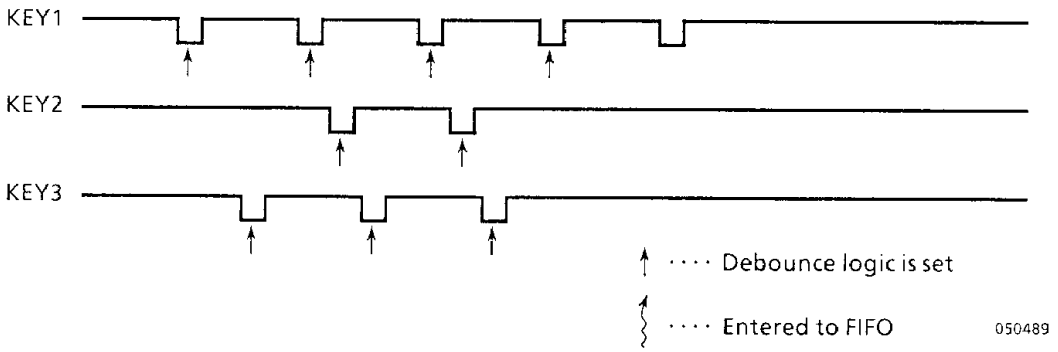

Figure 8.2 Example of a Case Where all Depressed Keys are Ignored

As shown in Figure 8.1 if all the other keys are released before the first depressed key, the first depressed key is recognized. As shown in Figure 8.2 if the first depressed key is released within one debounce cycle after the other keys was released, then all keys are ignored.

8.2 SCANNED KEYBOARD, N-KEY ROLLOVER

In this mode, each key depression is independently treated from all others. In the 2-key lockout mode, if a key is depressed, the debounce logic is set. If the other keys are depressed within one debounce cycle after it, the debounce logic is set again. The first depressed key is ignored. In the N-key Rollover mode, if a key is depressed waits one debounce cycle and then checks of the key is still down. If it is, the key is entered into the FIFO even of other keys are depressed.

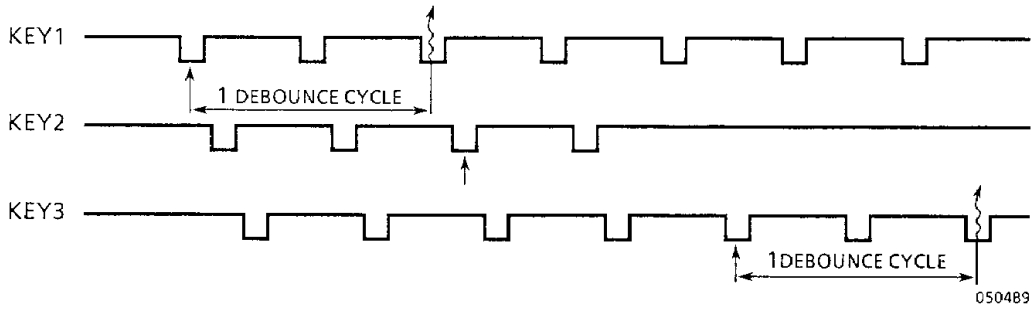

Figure 8.3 Example of 3 Keys Being Pushed Simultaneously

In the example as shown in Figure 8.3 the debounce circuit starts by Key 1, and checks if the key is still down after one debounce cycle. If it is, Key 1 is recognized and Key 2 is ignored not to be depressed for one debounce cycle.

8.3 SPECIAL ERROR MODE (N-KEY ROLLOVER)

This mode is set if the E bit of the End interrupt/error mode set command is programmed to "1". In the normal N-Key Rollover Mode, the key information is entered to the FIFO according to the key scan timing even if a simultaneous multiple depression occures during one debounce cycle. In the Special Error Mode, if a simultaneous multiple depression occurs during one debounce cycle, sets the error falg (the S/E bit of the FIFO status word) to "1". This flag prevents any further writing into the FIFO and will set interrupt request (IRQ). The S/E bit is cleared if the normal Clear command is written with CF = 1.

8.4 SENSOR MATRIX MODE

In Sensor Matrix Mode, the debounce circuit does not operate. The status of the sensor switch is inputted directly to the Sensor RAM. The MPU can only know a validated closure in the keyboard mode, however this mode has such advantage that the CPU knows how long the sensor was closed and when it was released. If there is any change in the sensor value at the end of the sensor matrix scan, the IRQ line goes high. The IRQ line is cleared by the first data read if the Auto-increment flag is "0" or by the End Interrupt/error mode set command if AI = 1.

8.5 STROBE INPUT MODE

In Strobe Input Mode, the debounce circuit does not operate. The data is inputted into the FIFO from the return lines at the rising edge of CNTL/STB Signal. When the data is entered into the FIFO, the IRQ line goes high. The functions of the FIFO and the FIFO status in this mode are same as those in the keyboard mode.

9. DATA FORMAT

9.1 KEYBOARD MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
CNTL	SHIFT	SCAN			RETURN		

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In this mode, the Data Format of the character entered into the FIFO is as follows. The MSB is the status of CNTL/STB line and the next MSB shows the status of SHIFT line. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

9.2 SENSOR MATRIX MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

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In this mode, the data on return lines is inputted in the row of the Sensor RAM in order according to the scan. The data is entered even if there is no change in the status of the sensor matrix switches. Each switch position maps to a Sensor RAM position. CNTL and SHIFT signals are ignored.

9.3 STROBE INPUT MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

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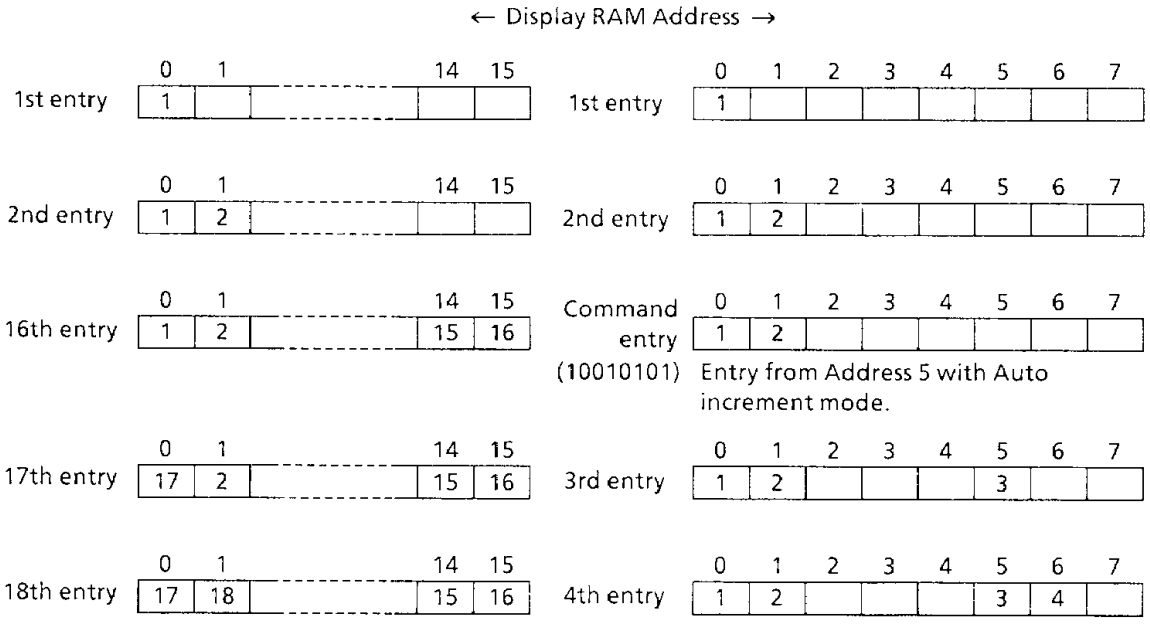
In this mode, the data on return lines is entered into FIFO at the rising edge of CNTL/STB signal.

10. INTERFACE WITH DISPLAY

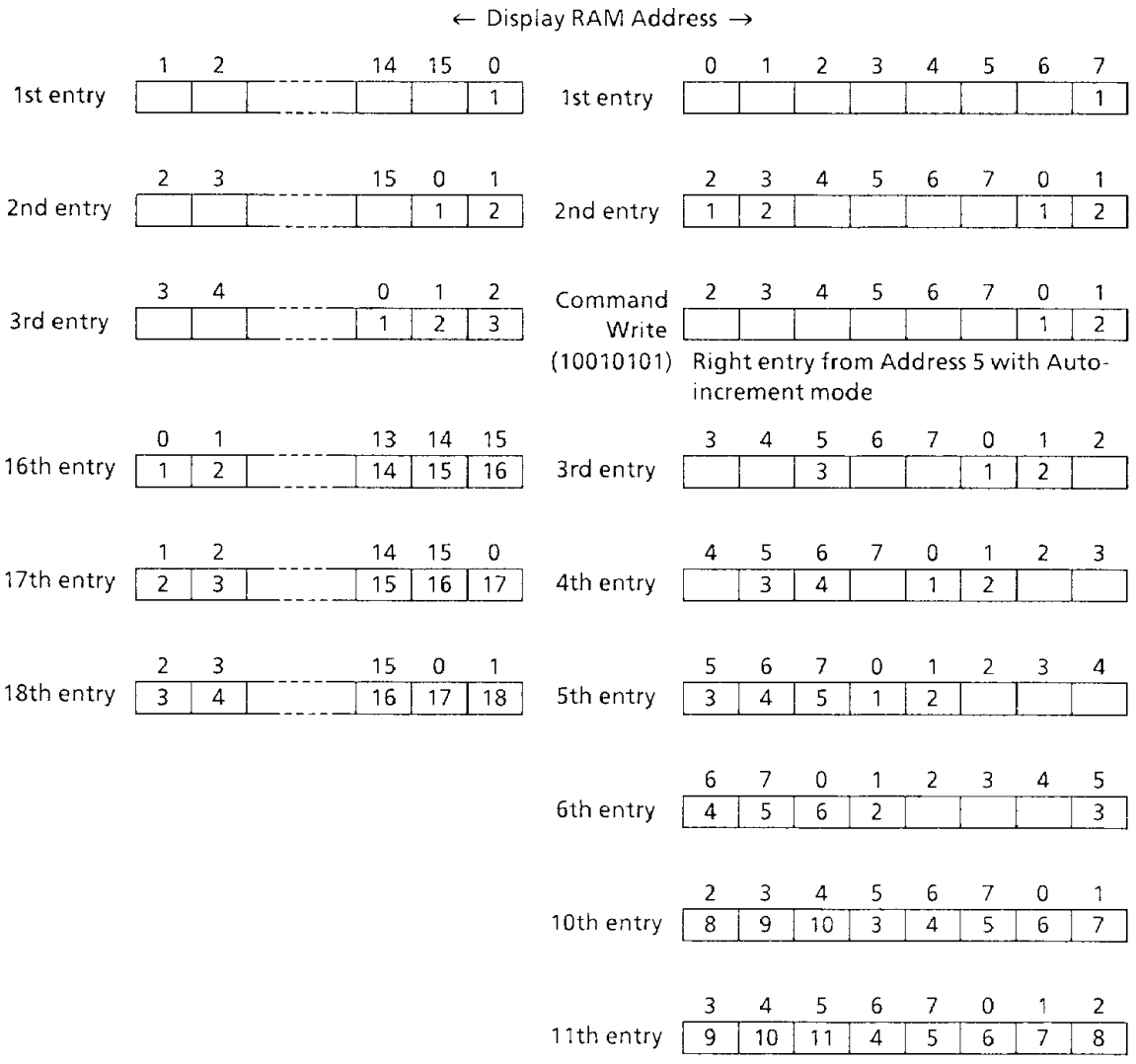
10.1 LEFT ENTRY

In Left Entry mode, address 0 of the Display RAM is the left-most side of the display and address 15 (address 7 in the case of 8-character display) is the right-most side. when characters are inputted onto the display RAM with the auto increment mode from address 0 of the display RAM, Characters are filled from the left-most position of the display. The 17th (or 9th) character is placed in the left-most position again. Address of the display RAM corresponds directly to each display positon of the display, and so its position does not change every entry.



10.2 RIGHT ENTRY

In Right Entry, the first entry is from the right-most position. Address of the Display RAM does not correspond to the display position.



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11. ELECTRIC CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	VCC Supply Voltage (with respect to VSS (GND))	− 0.5 to + 7.0	V
V_{IN}	Input Voltage (with respect to VSS (GND))	− 0.5 to VCC + 0.5	V
V_{OUT}	Output Voltage (with respect to VSS (GND))	− 0.5 to VCC + 0.5	V
P_D	Power Dissipation	250	mW
T_{sol}	Soldering Temperature (soldering time 10 sec)	260	°C
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_{opr}	Operating Temperature	− 40 to + 85	°C

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11.2 D.C. ELECTRICAL CHARACTERISTICS

(Ta = − 40 to + 85 °C, V_{CC} = 5V ± 10%, V_{SS} (GND) = 0V)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL1}	Input Low Voltage (RL_0-RL_7)		− 0.5	−	1.4	V
V_{IL2}	Input Low Voltage (Others)		− 0.5	−	0.8	V
V_{IH1}	Input High Voltage (RL_0-RL_7)		2.2	−	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage (Others)		2.2	−	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	IOL = 2.2mA	−	−	0.45	V
V_{OH1}	Output High Voltage	IOH = -400μA	2.4	−	−	V
V_{OH2}	Output High Voltage	IOH = -100μA	Vcc − 0.8	−	−	V
I_{IL1}	Input 1LEAK Current (SHIFT, CNTL, RL_0-RL_7)	VIN = VCC	−	−	+ 10	μA
		VIN = 2.4V	− 10	− 30	−	
		VIN = 0V	−	−	− 100	
I_{IL2}	Input Leak Current (Others)	0V ≦ VIN ≦ VCC	−	−	± 10	μA
I_{OFL}	Output Leak Current	0.45V ≦ VOUT ≦ VCC	−	−	± 10	μA
I_{CC}	Operating Supply Current	VIH = VCC-0.2V VIL = 0.2V, fc = 5MHz	−	−	5	mA

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11.3 INPUT CAPACITY

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capcity	fc = 1MHz Unmeasured Pins returned to VSS.	—	5	10	pF
C_{OUT}	Output Capcity		—	10	20	pF

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11.4 A.C. ELECTRICAL CHARACTERISTICS

Ta = − 40 to + 85° C, VCC = 5.0V ± 10%, VSS (GND) = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Set up Time ($\overline{RD}$)	10	—	—	ns
t_{RA}	Address Hold Time ($\overline{RD}$)	10	—	—	ns
t_{RR}	$\overline{RD}$ Pulse Width	160	—	—	ns
*t_{RD}	Valid Data ($\overline{RD}$)	—	—	120	ns
*t_{AD}	Address to Valid Data	—	—	185	ns
t_{DF}	Data Floating ($\overline{RD}$)	10	—	85	ns
t_{RCY}	Read cycle Time	200	—	—	ns
t_{AW}	Address Set up Time ($\overline{WR}$)	0	—	—	ns
t_{WA}	Address Hold Time ($\overline{WR}$)	0	—	—	ns
t_{WW}	$\overline{WR}$ Pulse Width	160	—	—	ns
t_{DW}	Data Set up Time ($\overline{WR}$)	120	—	—	ns
t_{WD}	Data Hold Time ($\overline{WR}$)	30	—	—	ns
t_{WCY}	Write Cycle Time	200	—	—	ns
t_{OWH}	CLK Pulse Width of High Level	80	—	—	ns
t_{OWL}	CLK Pulse Width of Low Level	50	—	—	ns
t_{CY}	Clock Period	200	—	—	ns

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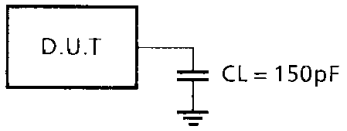
*TEST CONDITION CL = 150pF

11.4.1 AC TEST CONDITION



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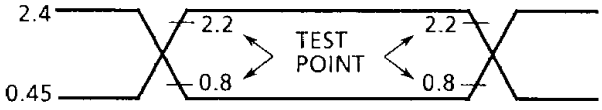
11.4.2 AC TEST INPUT WAVEFORM



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12. TIMING DIAGRAM

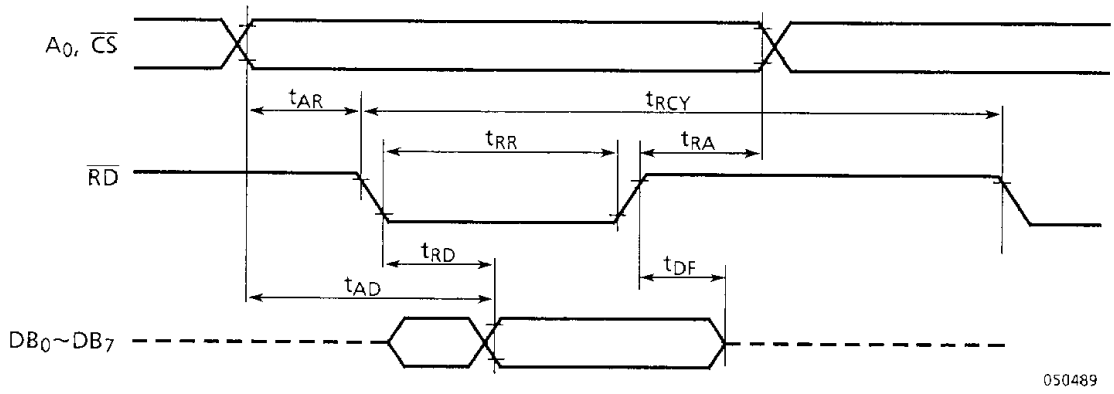


Figure 12.1 READ TIMING

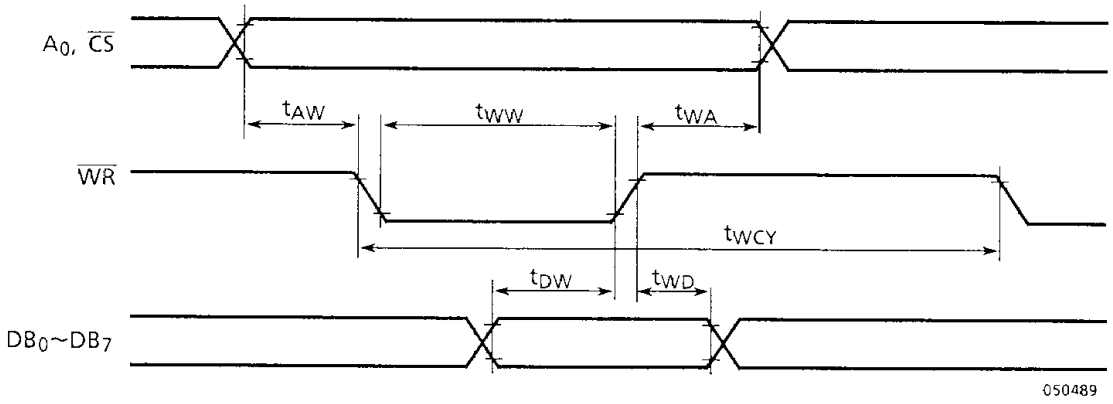


Figure 12.2 WRITE TIMING

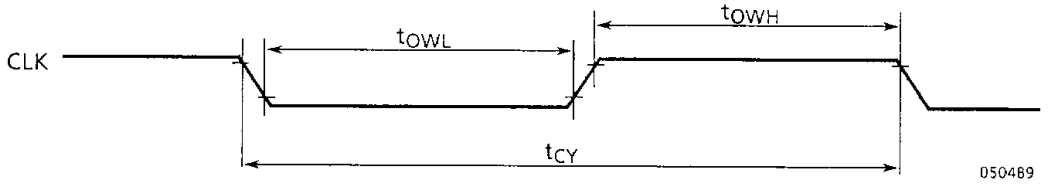


Figure 12.3 CLOCK TIMING

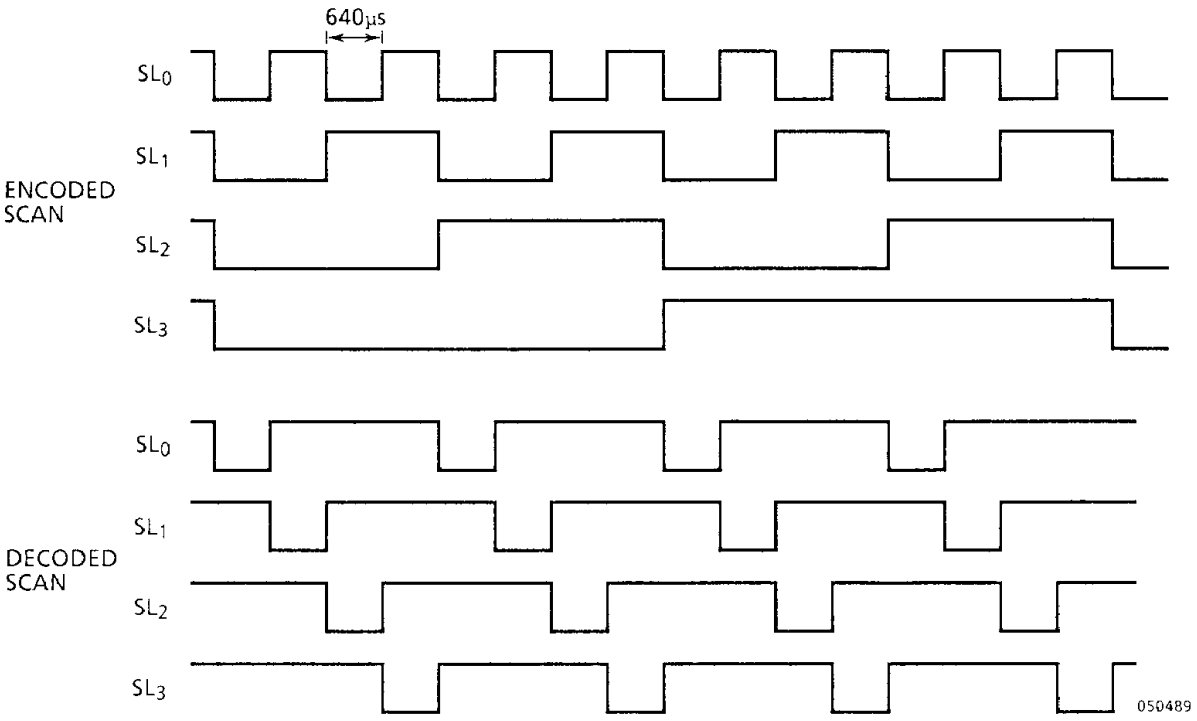


figure 12.4 scan timing

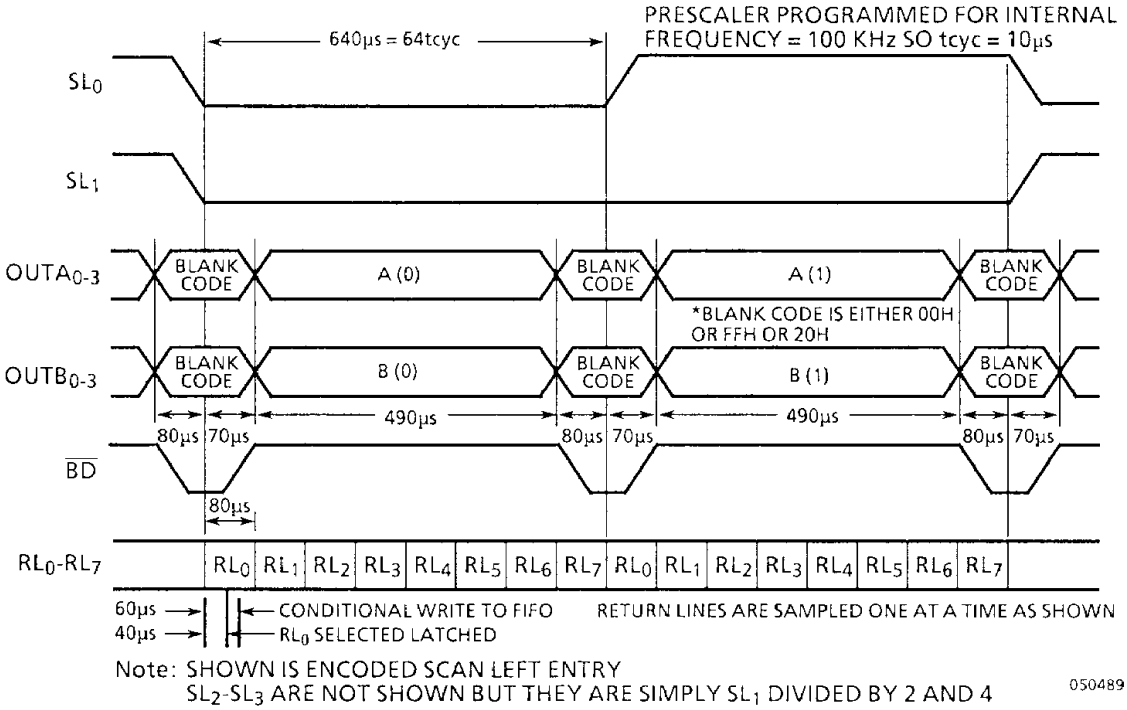


figure 12.5 example of display timing

13. EXAMPLE OF APPLICATION CIRCUIT

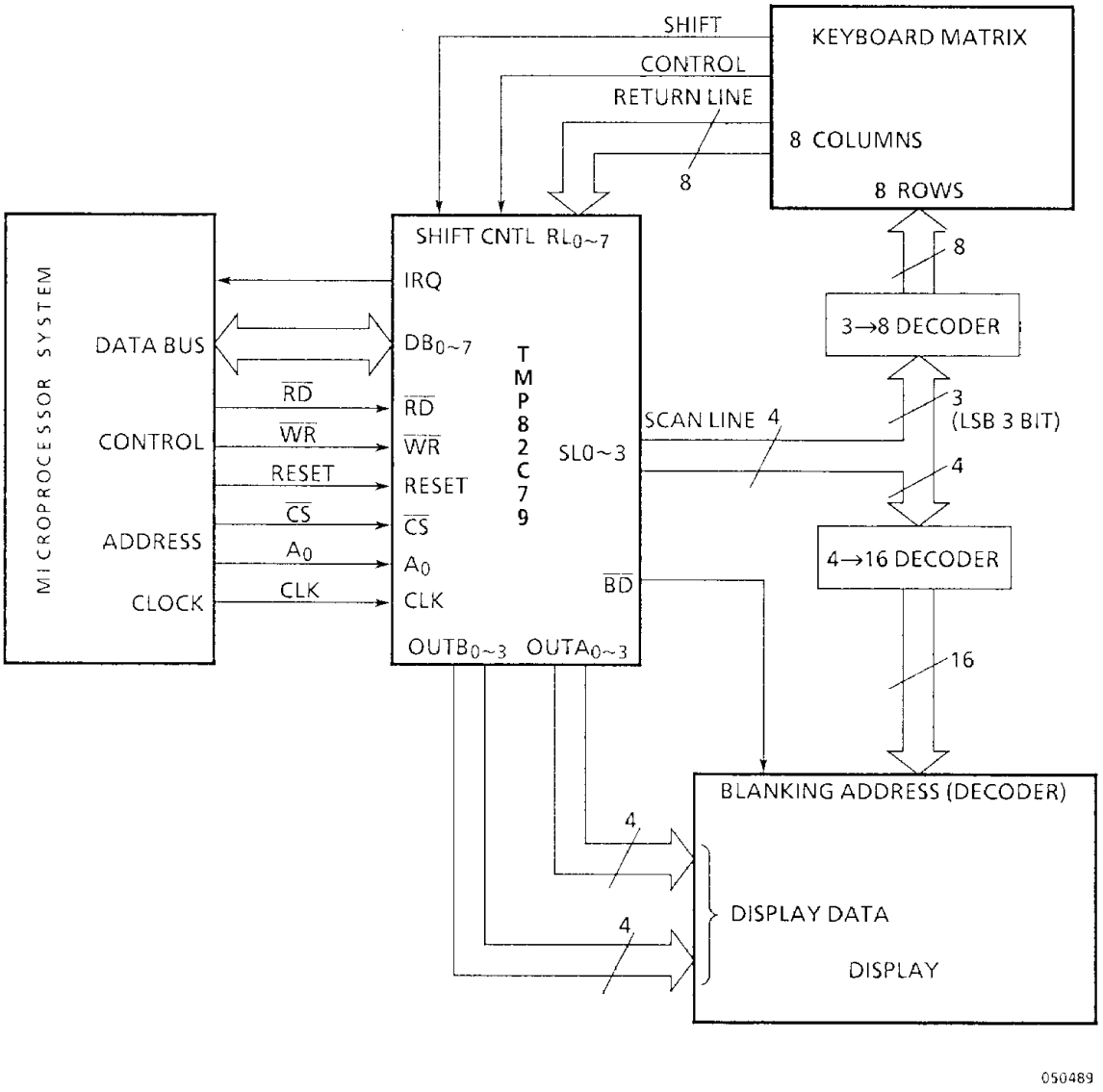


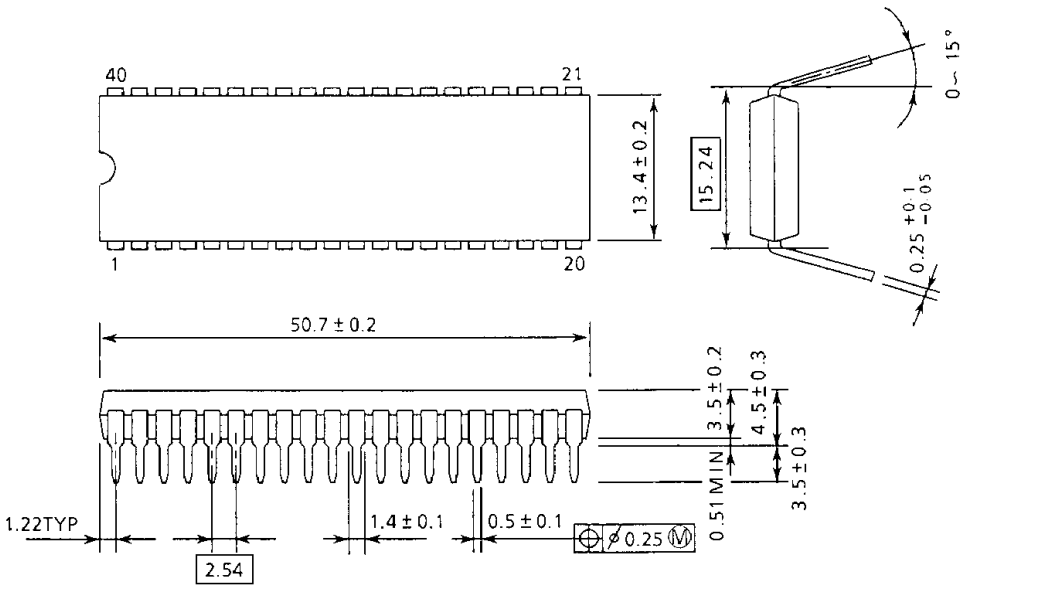
Figure 13.1 EXAMPLE OF APPLICATION CIRCUIT

14. EXTERNAL DIMENSION

14.1 40PIN DIP EXTERNAL DIMENSION

DIP40-P-600

Unit : mm



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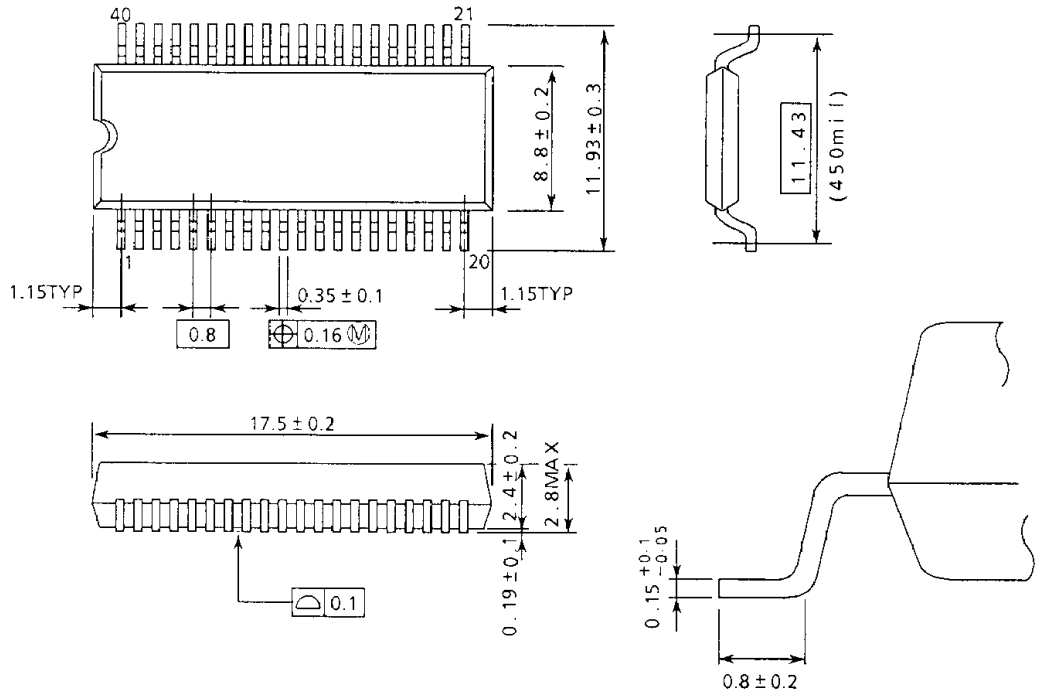
Note : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

14.2 40PIN SOP EXTERNAL DIMENSION

SSOP40-P-450

Unit : mm



Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

TMP8279P-5

1. GENERAL DESCRIPTION

The TMP8279P-5 (hereinafter referred to as TMP8279) is a programmable keyboard/display interface designed for use as the TLCS-85A microcomputer peripheral. The keyboard portion can provide a scanned interface to a 64-contact key matrix. Also, the keyboard portion can interface to an array of sensors or a strobed interface keyboard. Key depressions can be 2-key lockout or N-key rollover. The display portion has 16×8 bits display RAM which can be treated as dual 16×4 bits. Both right entry and left entry display formats are possible.

2. FEATURES

- Simulataneous Keyboard/Display operation is possible
- Scanned Keyboard mode.
- Scanned Sensor Matrix mode.
- Strobed Input Entry mode.
- Buil in 8-character FIFO or 64 bit Sensor RAM
- Programmable 2 Key Lockout or N-key Rollover with contact Debounce.
- Built in 16×8 bit display RAM.
- Programmable scan timing
- Compatible with INTEL 8279-5.

3. PIN CONNECTION

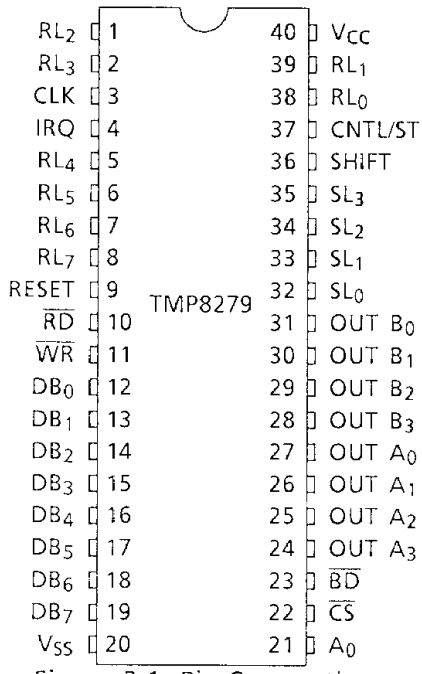


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Figure 3.1 Pin Connection

4. BLOCK DIAGRAM

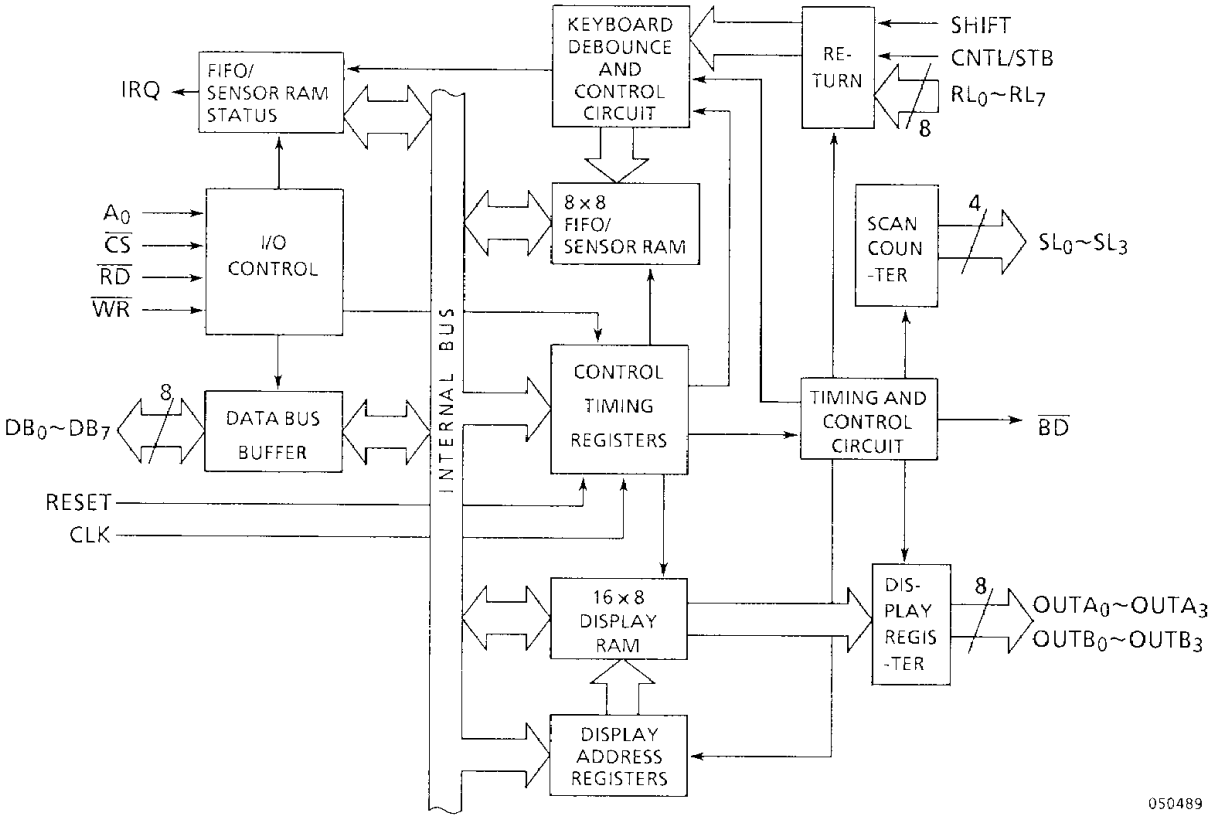

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Figure 4.1 Block Diagram

5. PIN NAME AND PIN DESCRIPTION

- VSS (Power Supply)

  Ground

- VCC (Power Supply)

  +5V during operaiton

- DB_0~DB_7 (Input/Output)

  Bidirecitonal Data Bus. All data and commands are transfered via this data bus.

- CLK (Input)

  System clock used to generate the TMP8279 internal timing.

- RESET (Input)

  A high level signal on this pin resets the TMP8279. After being reset the TMP8279 is placed in the following state.

  (1) 16×8 bit character display, left entry.

  (2) Encode scan keyboard, 2 key lockout, clock pre-scale value is set to 31.

- $\overline{CS}$ (Input)

  A low level input on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the MPU and the TMP8279.

- A_0 (Input)

  This inputs acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. A high level input on this pin indicates the signals on data bus are interpreted as command or status. A low level input indicates they are data in the RAMs.

- $\overline{WR}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP8279 to accept command or data from the MPU.

- $\overline{RD}$ (Input)

  A low level input on this pin when $\overline{CS}$ is low enables the TMP8279 to output data or status onto the bus.

- IRQ (Output)

  Interrupt request output. In a keyboard mode, the interrupt line is high when the FIFO/Sensor RAM has effective data. The interrupt line goes low when each FIFO/Sensor RAM read and returns high if the RAM still has effective data. In sensor matrix mode, the interrupt line goes high whenever any change in the sensor matrix is detected.

- SL_0~SL_3 (Output)

  Scan lines which are used to scan the key switch or the sensor matrix and the display digits. These lines can be either encoded (1 of 16) of decode (1 of 4).

- RL_0~RL_7 (Input)

  Return lines which are connected to the scan lines through the keys or sensor switches. Each line has an internal pullup to keep it high until a switch closure pulls it low. They also serve as an 8-bit input in Strobed Input mode.

- SHIFT (Input)

  This input status is stored in the FIFO RAM in addition to information of the key position on key closure in Scannned key board modes. It has an internal pullup to keep it high until a switch closure pulls it low.

- CNTL/STB (Input)

  For Keyboard modes this line is used as a control input and stored like status on a key closure. This can be programmed as the strobe line that enters the data into FIFO in Strobed Input mode (Rising Edge). It has an internal pullup to keep it high until a switch closure pulls it low.

- $OUTA_0$~$OUTA_3$ (Output)

- $OUTB_0$~$OUTB_3$ (Output)

  These two ports are the outputs for the 16×4 display refresh registers. The data from these outputs is updated synchronized with the scan lines (SL_0~SL_3) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be treated as one 8-bit port.

- $\overline{BD}$ (Output)

  This output is used to blank the display during digit switching or by a display blanking command.

6. FUNCTIONAL DESCRIPTION

6.1 I/O CONTROL AND DATA BUS BUFFER

The I/O control section uses the $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$ lines and controls the flow of data to and from the various internal registers and buffers in the TMP8279. $\overline{CS}$ input enables the all data flow to and from the TMP8279. The character of the information given by the MPU, is identified by A_0. $\overline{RD}$ and $\overline{WR}$ decide the direction of data flow through the data bus buffer. The data bus buffer is bidirectional buffer which is used for connecting the internal bus and a system bus. When $\overline{CS}$ is high, the buffer is in a high impedance state.

6.2 CONTORL REGISTER, TIMING REGISTER AND TIMING CONTROL CIRCUIT

The keyboard and display modes or the other operating conditions are programmed by the MPU. These modes are latched at the rising edge of $\overline{WR}$ when A_0 is high. The timing control contains the basic counter chains. The first counter is the 1/N prescaler that can be programmed to yield an basic internal frequency which gives a 5.1ms keyboard scan time and a 10.3ms debounce time. The other counters divide down the basic internal frequency to provide the proper keyboard matrix scan and display scan timings.

6.3 SCAN COUNTER

Two modes are available for the scan counter. In the encode mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the key board and display. In the decode mode, the scan counter decodes the least significant 2 bits internally and provides a decoded 1 of 4 scan. Note that the only first 4 characters in the Display RAM are outputted from $OUTA_{0\text{-}3}$ and $OUTB_{0\text{-}3}$ in the decode mode.

6.4 RETURN BUFFER AND KEYBOARD DEVOUNCE CONTROL CIRCUITS

The 8 return lines are latched onto the return line buffer. In the Keyboard mode, these lines are scanned to look for key closures in a row. If the debounce circuit detects a closed switch, it waits about 10ms*, and checks if the switch remains closed. If it does so, the address of the switch and the status of SHIFT and CNTL lines is transferred to the FIFO .

6.5 FIFO/SENSOR RAM AND FIFO/SENSOR RAM STATUS

The FIFO/Sensor RAM is a dual funciton RAM. In the keyboard mode or in the Strobe Input mode, this RAM serves as a FIFO. The FIFO status shows whether the FIFO is empty or full and keeps the number of characters in the FIFO. In addiiton, there is a flag to show an error in the case where too many reads or writes is recognized. The FIFO status can be read at $\overline{CS}=\overline{RD}=0$, $A_0=1$. The FIFO status logic provides an IRQ signal when the FIFO is not empty. In the scanned sensor matrix mode, the RAM serves as a Sensor RAM. IRQ becomes high when a change in the sensor is detected.

6.6 DISPLAY ADDRESS REGISTERS AND DISPLAY RAM

The display address registers hold the address of the word currently being written or read by the MPU and the two 4 bit nibbles being displayed. The Display RAM stores data for display outputs. The read/write addresses are programmed by the MPU command. They also can be programmed to auto-increment after read or wirte. The Display RAM can be directy read out by the MPU after mode and address is set. The A and B nibbles of the Display RAM are outputted to the Display Outputs A and B syncronously with scan signals (SL_0~SL_3). The A and B nibbles can be entered independently or as one word by the MPU command.

* In case of 100KHz basic internal frequency.

7. COMMAND DESCRIPTION

7.1 KEYBOARD/DISPLAY MODE SET

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	0	D	D	K	K	K

Display Mode

0	0	8 × 8 bit character display – Left entry
* 0	1	16 × 8 bit character display – Left entry
1	0	8 × 8 bit character display – Right entry
1	1	16 × 8 bit character display – Right entry

* Default after reset

Keyboard Mode

* 0	0	0	Encoded Scan Keyboard – 2-Key Lockout
0	0	1	Decoded Scan Keyboard – 2-Key Lockout
0	1	0	Encoded Scan Keyboard – N-Key Rollover
0	1	1	Decoded Scan Keyboard – N-Key Rollover
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

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7.2 PROGRAM CLOCK

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	0	1	P	P	P	P	P

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The TMP8279 generates all timing and multiplexing signals by means of the internal prescaler. The prescaler generates internal reference clocks by dividing an external supply clock by a programmable value PPPPP. Any number from 2 to 31 can be set as a prescaler value. When this value is set to 0 or 1, it is interpreted to be 2. If the internal reference clock is set to 100kHz, it is possible to obtain 5.1ms keyboard scan time and 10.3ms debounce time. The value PPPPP is set to 31 after reset, but cannot be changed by the Clear command.

7.3 READ FIFO/SENSOR RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	0	AI	X	A	A	A

X = don't care

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If this command is writen, the subsequent data reads are set up for the FIFO/Sensor RAM. Auto-increment flag (AI) and the RAM address bits AAA are valid only in Sensor Matrix Mode. The address bits AAA select one of the 8 rows of the Sensor RAM. If AI=1, the RAM address is incremented after each successive read. The Auto-incremented flag does not affect the auto-increment of the Display RAM.

7.4 READ DISPLAY RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
0	1	1	AI	A	A	A	A

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If this command is written, the subsequent data reads are set up for the Display RAM. The address bits AAAA select one of the 16 rows of the Display RAM. If AI=1, the address is incremented after each read or write to the Display RAM. This command sets the next read or write address and the sense of the Auto-increment.

7.5 WRITE DISPLAY RAM

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	AI	A	A	A	A

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If this command is written, the subsequent data writes are set up for the Display RAM. Note that writing this command does not switch the source of the subsequent data reads. The address register of the Display RAM is same for read/write operations. The addressing and Auto-increment funciton are identical to those for the Read Display RAM.

7.6 DISPLAY WRITE INHIBIT/BLANKING

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	1	X	IWA	IWB	BLA	BLB

X = don't care

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The IWA or IWB bit can be used to mask A nibble or B nibble for entering the Display data independently. The BLA or BLB flag is available for the nibble A or B to blank the display. In the case where the Display Outputs are used as separate 4-bit display ports, the IWA or IWB bit is useful so as not to affect the other display port when the MPU writes a word to the display RAM. The BLA or BLB bit is used for blanking the display independently without giving any affect to the other 4-bit display port. The blank code is determined by the last Clear command that has been programmed after reset. If the Display Output is used as an 8-bit port, it is necessary to set both BLA and BLB bits for blanking the display. The $\overline{BD}$ signal becomes low.

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
↕	↕	↕	↕	↕	↕	↕	↕
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0

Correspondence between Display Output and Data Bus

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7.7 CLEAR

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	1	0	C_D	C_D	C_D	C_F	C_A

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The C_D bits are used to clear all rows of the Dislay RAM to the following code shown below.

(DB_4) C_D	(DB_3) C_D	(DB_2) C_D	
1	0	×	···· All Zeros (X = Don't Care)
1	1	0	···· All Hex 20H (0010 0000)
1	1	1	···· All Ones
0	×	×	···· not clear display if $C_A = 0$

Enable clear display when $C_D = 1$ (or by $C_A = 1$)

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While the Display RAM is being cleared, it may not write to the Display RAM. The MSB bit of the FIFO status word is set during this time. If the C_F bit is set to "1", the FIFO status is cleared and the interrupt request output (IRQ) is reset. Also, the Sensor RAM pointer is set to the row 0.

The C_A bit has the combined effect of the C_D bit and C_F bit. It enables clear display code to the Display RAM and also clears the FIFO status. Furthermore, it re-synchronizeds the inernal timing chains.

7.8 END INTERRUPT/ERROR MODE SET

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	1	1	E	×	×	×	×

X: don't care

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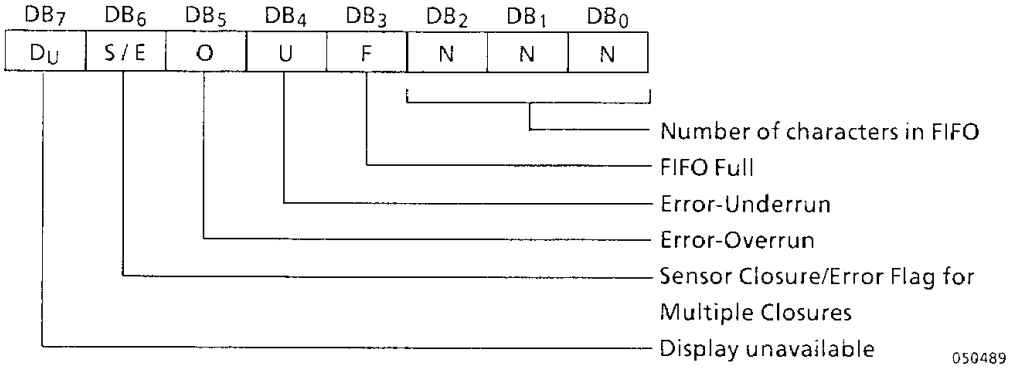
In the Sensor Matrix mode, this command loweres the IRQ line and enables writing to the Sensor RAM. This means that a write to the Sensor RAM is inhibited when IRQ line is high. If the E bit is set to "1", the S/E bit of the FIFO status becomes "1" when any one of the sensor switches is closed. If E = 0, the S/E bit is always "0". In the N-Key Rollover, if the E bit is progrmamed to "1", the Special Error mode will be resulted.

7.9 FIFO STATUS



Du : indicates that the Display RAM is unavailable because a Clear Display or Clear All command has not completed its clearing operation.

S/E : in a Sensor Matrix mode, if the E bit of End Interrupt/Error Mode Set is programmed to "1", this S/E bit is set to indicate that at least one sensor closure indication is contained in the Sensor RAM.
In Special Error Mode, this S/E bit is showing the error flag and serves as an indication to whether a simulataneous multiple closure error has occured.

O : indicates that the entry of another character into a full FIFO was attempted.

U : indicates that the MPU tried to read an empty FIFO.

F : indicates that the FIFO is full of the eight characters.

NNN : indicate number of characters in the FIFO when in the Keyboard Mode or in the Strobe Input Mode.

Table 7.1 Addressing

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Functions
0	0	0	1	Read Data
0	0	1	0	Write Data
0	1	0	1	Read Status word
0	1	1	0	Write Command word
1	×	×	×	High-impedance state

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8. INTERFACE WITH KEYBOARD

8.1 SCANNED KEYBOARD, 2-KEY LOCKOUT

In this mode, if one key only is kept depressed during one debounce cycle (2 times of the key scan cycle), the key is recognized. When a key is depressed, the debounce logic is set and the other depressed keys are checked during the next two scan cycle. If none are encountered, it is a single key depressing and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If another depressed key are encountered, operates as follows.

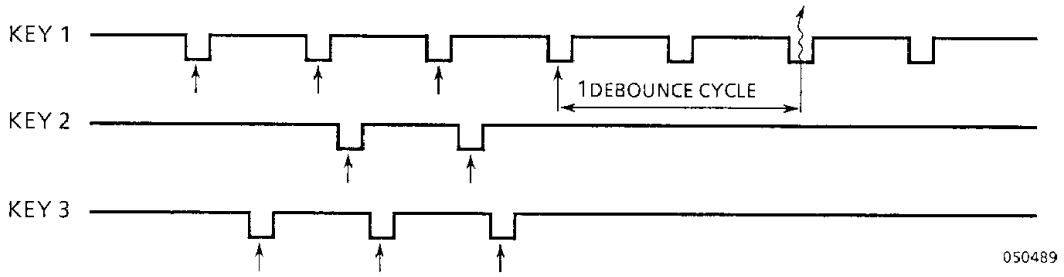

Figure 8.1 Example of a case where a first depressed key is continuously kept to the last

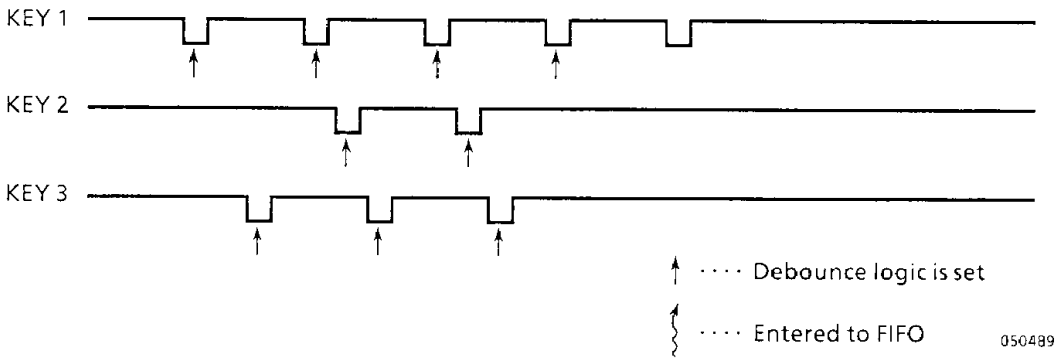

Figure 8.2 Example of a case where all depressed keys are ignored

As shown in Figure 8.1, if all the other keys are released before the first depressed key, the first depressed key is recognized. As shown in Figure 8.2, if the first depressed key is released within one debounce cycle after the other keys was released, than all keys are ignored.

8.2 SCANNED KEYBOARD, N-KEY ROLLOVER

In this mode, each key depression is independently treated from all others. In the 2-Key lockout mode, if a key is depressed, the debounce logic is set. If the other keys are depressed within one debounce cycle after it, the debounce logic is set again. The first

depressed key is ignored. In the N-key Rollover mode, if a key is depressed waits one debounce cycle and then checks if the key is still down. If it is, the key is entered into the FIFO even if other keys are depressed.

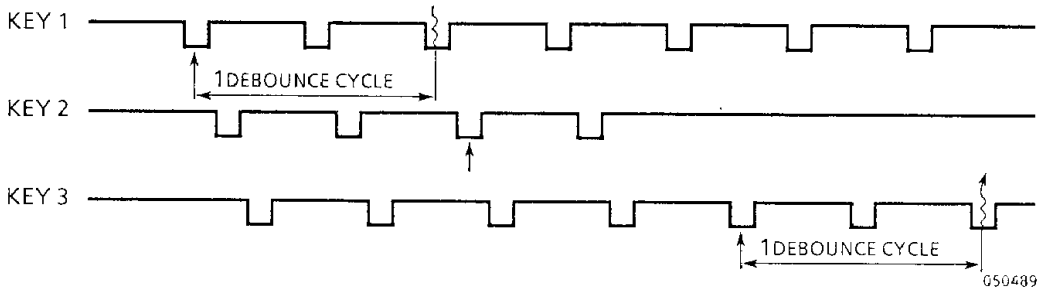

Figure 8.3 Example of 3 keys being pushed simultaneously

In the example as shown in Figure 8.3, the debounce circuit starts by Key 1, and checks if the key is still down after one debounce cycle. If it is, Key 1 is recognized and Key 2 is ignored not to be depressed for one debounce cycle.

8.3 SPECIAL ERROR MODE (N-KEY ROLLOVER)

This mode is set if the E bit of the End Interrupt/error Mode Set command is programmed to "1". In the normal N-Key Rollover Mode, the key information is entered to the FIFO according to the key scan timing even if a simulataneous multiple depression occures during one debounce cycle. In the Special Error Mode, if a simulataneous multiple depression occurs during one debounce cycle, sets the error flag (the S/E bit of the FIFO status word) to "1". This flag prevents any further writing into the FIFO and will set interrupt request (IRQ). The S/E bit is cleared if the normal Clear command is written with $C_F = 1$.

8.4 SENSOR MATRIX MODE

In Sensor Matrix Mode, the debounce circuit does not operate. The status of the sensor switch is inputted directly to the Sensor RAM. The MPU can know a validated closure in the keyboard, however this mode has such advantage that the MPU knows how long the sensor was closed and when it was released.

If there is any change in the sensor value at the end of the sensor matrix scan, the IRQ line goes high. The IRQ line is cleared by the first data read if the Auto-increment flag is "0" or by the End Interrupt/Error Mode Set command if AI = 1.

8.5 STROBE INPUT MODE

In Strobe Input Mode, the debounce circuit does not operate. The data is inputted into the FIFO from the return lines at the rising edge of CNTL/STB Signal. When the data is entered into the FIFO, the IRQ line goes high.

The functions of the FIFO and the FIFO status in this mode are same as those in the keyboard mode.

9. DATA FORMAT

9.1 KEYBOARD MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
CNTL	SHIFT	SCAN			RETURN		

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In this mode, the Data Format of the character entered into the FIFO is as follows. The MSB is the status of CNTL/STB line and the next MSB shows the status of SHIFT line. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

9.2 SENSOR MATRIX MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

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In this mode, the data on return lines is inputted in the row of the Sensor RAM in order according to the scan. The data is entered even if there is no change in the status of the sensor matrix switches. Each switch position maps to a Sensor RAM position. CNTL and SHIFT signals are ignored.

9.3 STROBE INPUT MODE

DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

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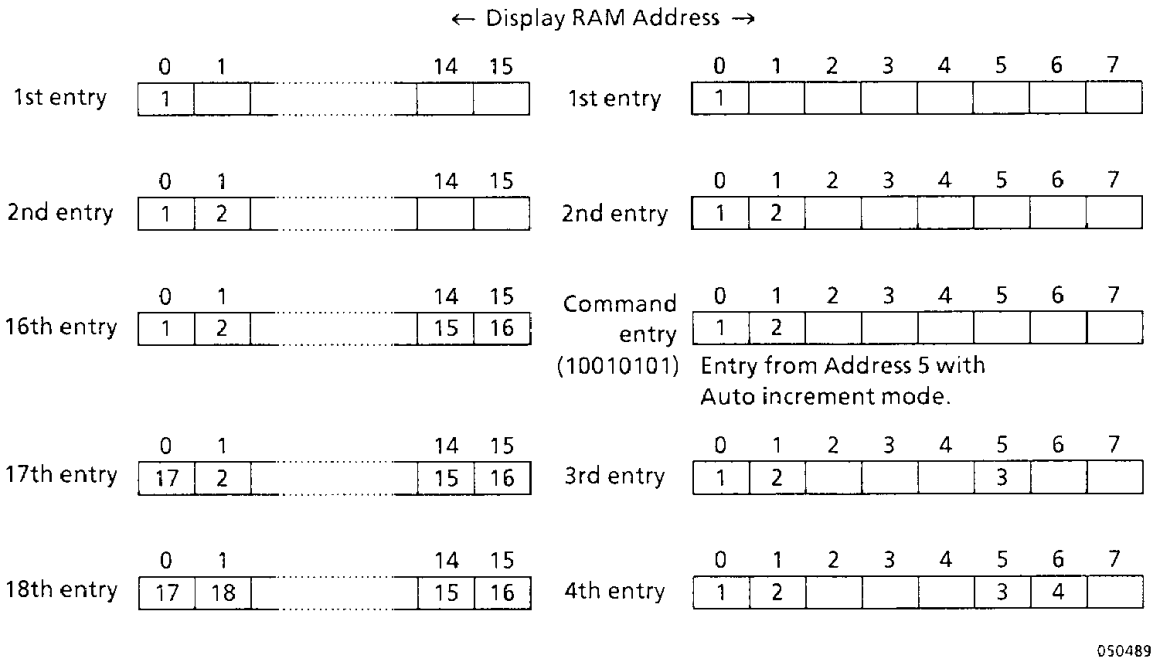
In this mode, the data on the return line is entered into the FIFO at the rising edge of CNTL/STB signal.

10. INTERFACE WITH DISPLAY

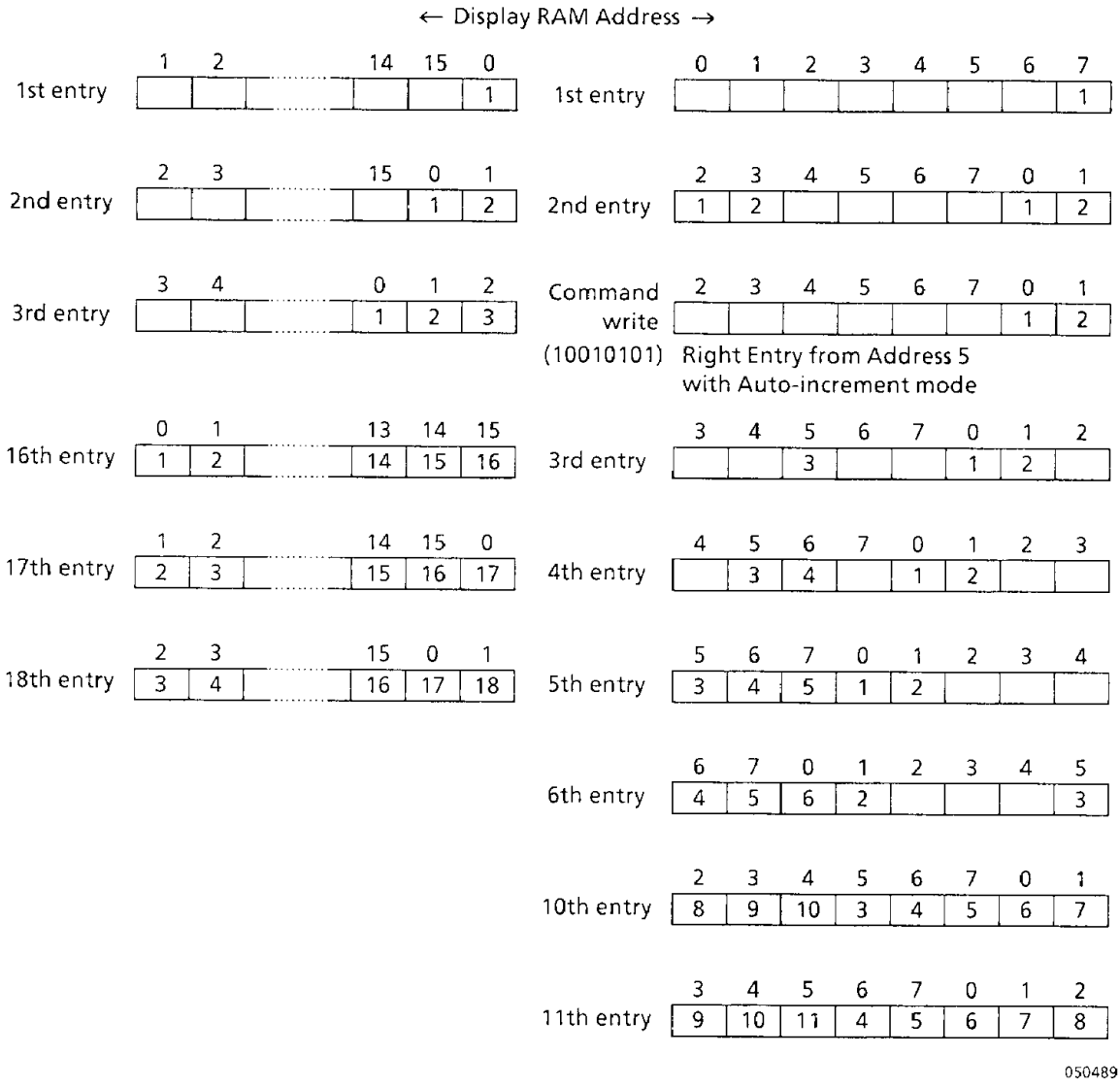
10.1 LEFT ENTRY

In Left Entry mode, address 0 of the Display RAM is the left-most side of the display and address 15 (address 7 in the case of 8-character display) is the right-most side. When characters are inputted onto the Display RAM with the auto-increment mode from address 0 of the display RAM, Characters are filled from the left-most position of the display. The 17th (or 9th) character is placed in the left-most position again. Address of the display RAM corresponds directly to each display position of the display, and so its position does not change every entry.



10.2 RIGHT ENTRY

In Right Entry, the first entry if from the right-most position. Address of the Display RAM does not correspond to the display position.



11. ELECTRIC CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Supply Voltage (with respect to GND (V_{SS}))	− 0.5 to + 7.0	V
V_{IN}	Input Voltage (with respect to GND (V_{SS}))	− 0.5 to + 7.0	V
V_{OUT}	Output Voltage (with respect to GND (V_{SS}))	− 0.5 to + 7.0	V
P_D	Power Dissipation	1	W
T_{sol}	Soldering Temperature (soldering time 10 sec)	260	°C
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_{opr}	Operating Temperature	0 to 70	°C

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11.2 D.C. ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL1}	Input Low Voltage (RL_0~RL_7)		− 0.5		1.4	V
V_{IL2}	Input Low Voltage (Others)		− 0.5		0.8	V
V_{IH1}	Input High Voltage (RL_0~RL_7)		2.2			V
V_{IH2}	Input High Voltage (Others)		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 2.2mA			0.45	V
V_{OH1}	Output High Voltage (IRQ)	I_{OH} = − 100μA	3.5			V
V_{OH2}	Output High Voltage (Others)	I_{OH} = − 400μA	2.4			V
I_{IL1}	Input Leak Current (SHIFT, CNTL, RL_0~RL_7)	V_{IN} = V_{CC}			+ 10	μA
		V_{IN} = 0V			− 100	
I_{IL2}	Input Leak Current (Others)	0V ≦ V_{IN} ≦ V_{CC}			± 10	μA
I_{OFL}	Output Leak Current	0.45V ≦ V_{OUT} ≦ V_{CC}			± 10	μA
I_{CC}	Supply Current				120	mA

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11.3 INPUT CAPACITY

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacity	f_C = 1MHz Unmeasured Pins returned to V_{SS}.		5	10	pF
C_{OUT}	Output Capacity			10	20	pF

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11.4 A.C. ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 5.0V ± 10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AR}	Address Set up Time ($\overline{RD}\downarrow$)		0			ns
t_{RA}	Address Set up Time ($\overline{RD}\uparrow$)		0			ns
t_{RR}	$\overline{RD}$ Pulse Width		250			ns
t_{RD}	Valid Data ($\overline{RD}\uparrow$)	C_L = 150pF			150	ns
t_{AD}	Address to Valid Data	C_L = 150pF			250	ns
t_{DF}	Data Floating ($\overline{RD}\uparrow$)		10		100	ns
t_{RCY}	Read Cycle Time		1			μs
t_{AW}	Address Set up Time ($\overline{WR}\downarrow$)		0			ns
t_{WA}	Address Hold Time ($\overline{WR}\uparrow$)		0			ns
t_{WW}	$\overline{WR}$ Pulse Width		250			ns
t_{DW}	Data Set up Time ($\overline{WR}\uparrow$)		150			ns
t_{WD}	Data Hold Time ($\overline{WR}\uparrow$)		0			ns
t_{OW}	CLK Pulse Width		120			ns
t_{CY}	Clock period		320			ns

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12. TIMING DIAGRAM

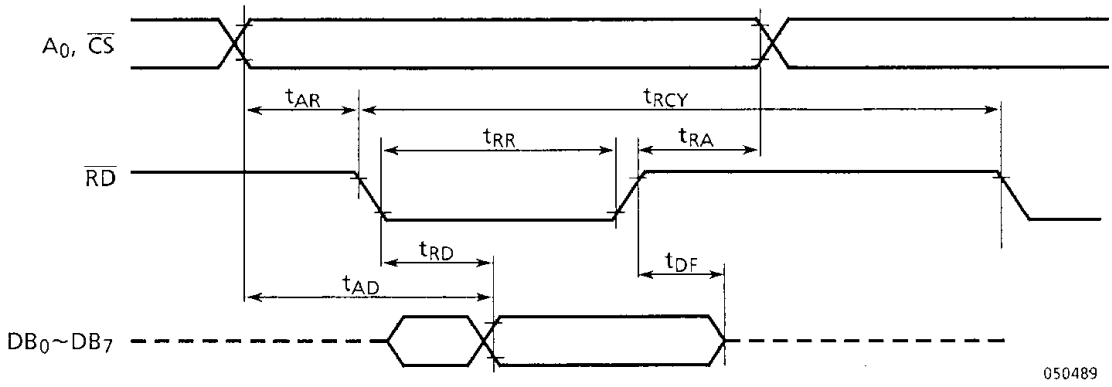


Figure 12.1 Read Timing

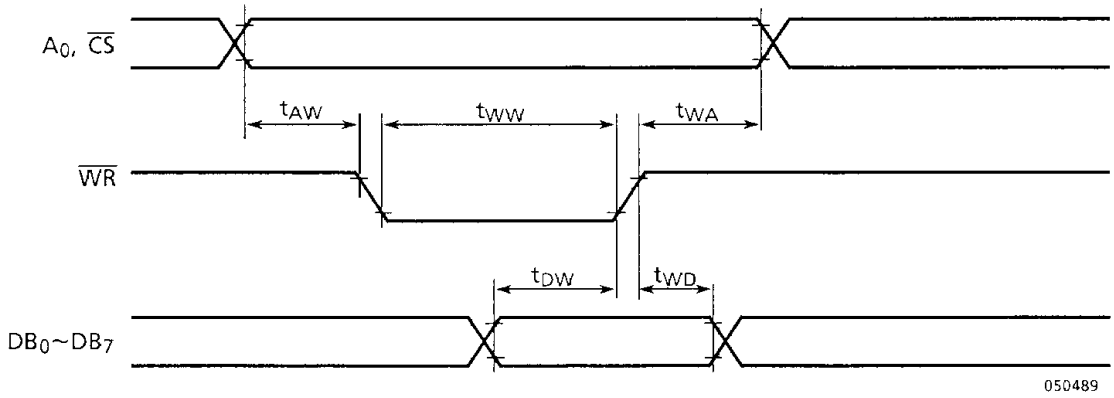


Figure 12.2 Write Timing

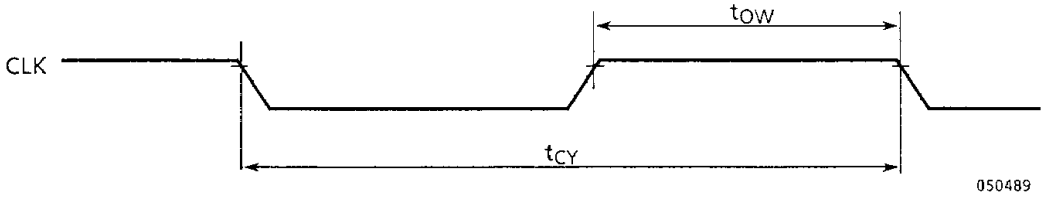


Figure 12.3 Clock Timing

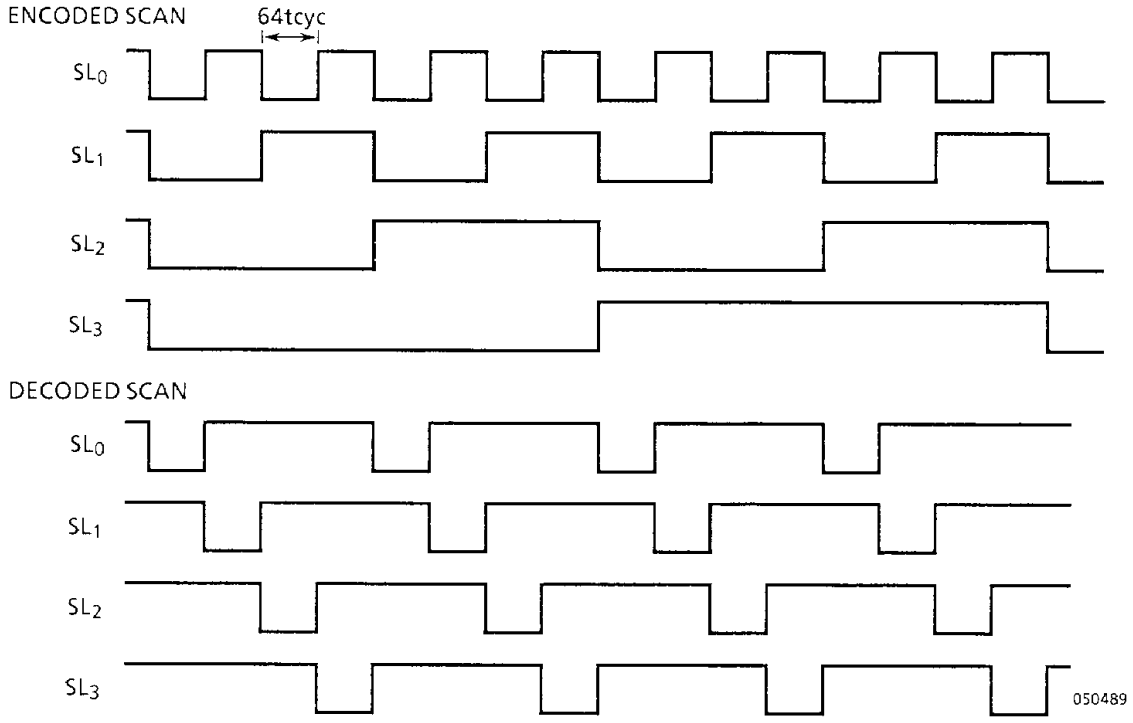
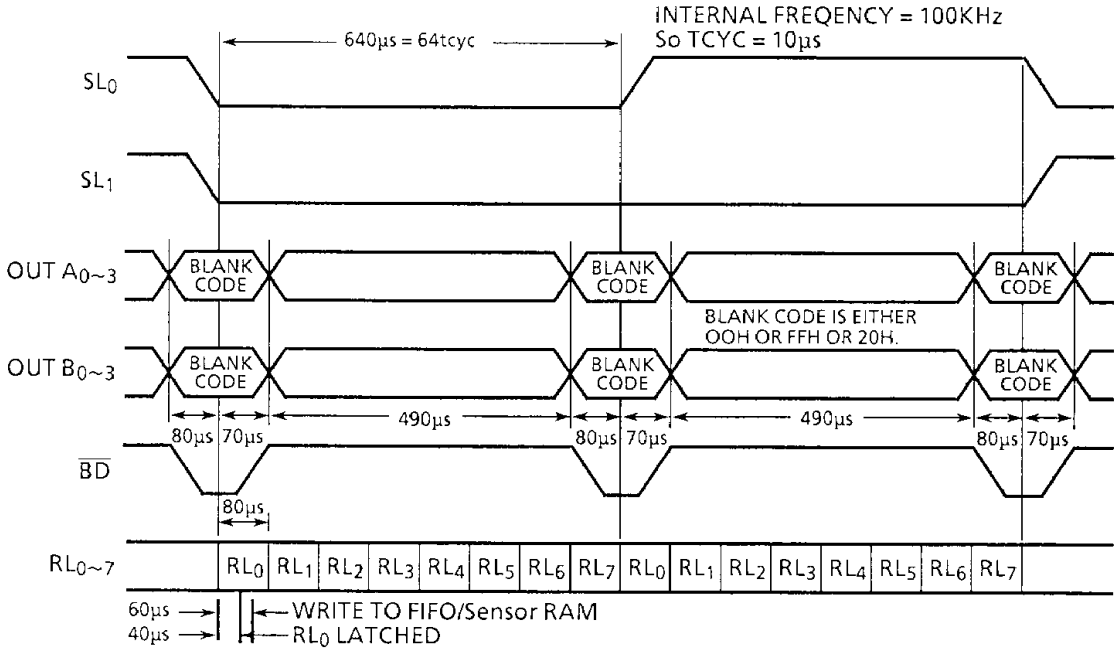


Figure 12.4 Scan Timing



Note : Shown is encoded scan, left entry SL2, SL3 are SL1 divided by 2 and 4. 050489

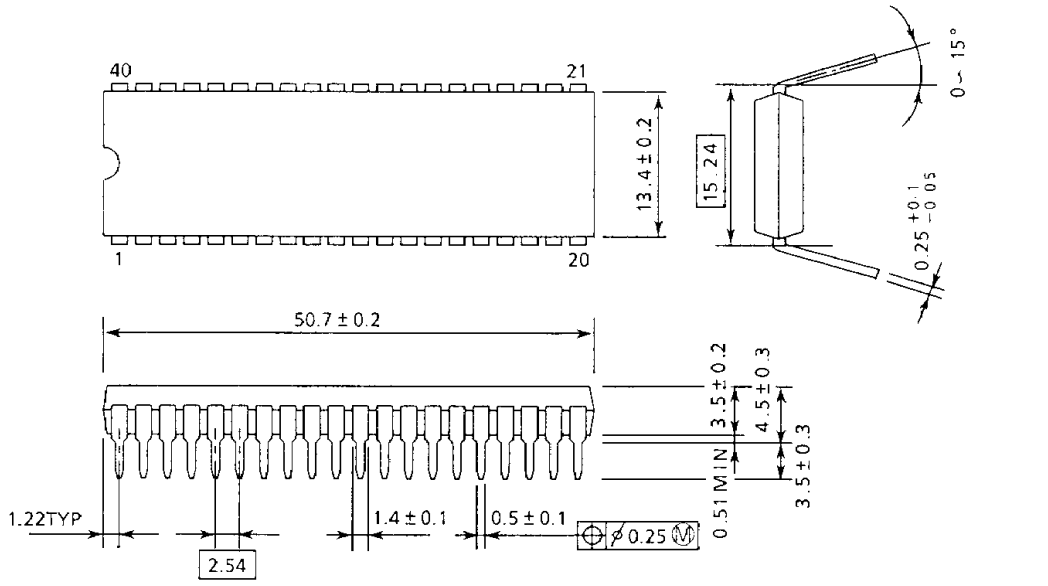
Figure 12.5 Example of Display

13. EXTERNAL DIMENSION

13.1 40 PIN DIP EXTERNAL DIMENSION

DIP40-P-600

Unit : mm



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Note: Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoritical positions with respect to No.1 and No.40 leads.

14. EXAMPLE OF APPLICATION CIRCUIT

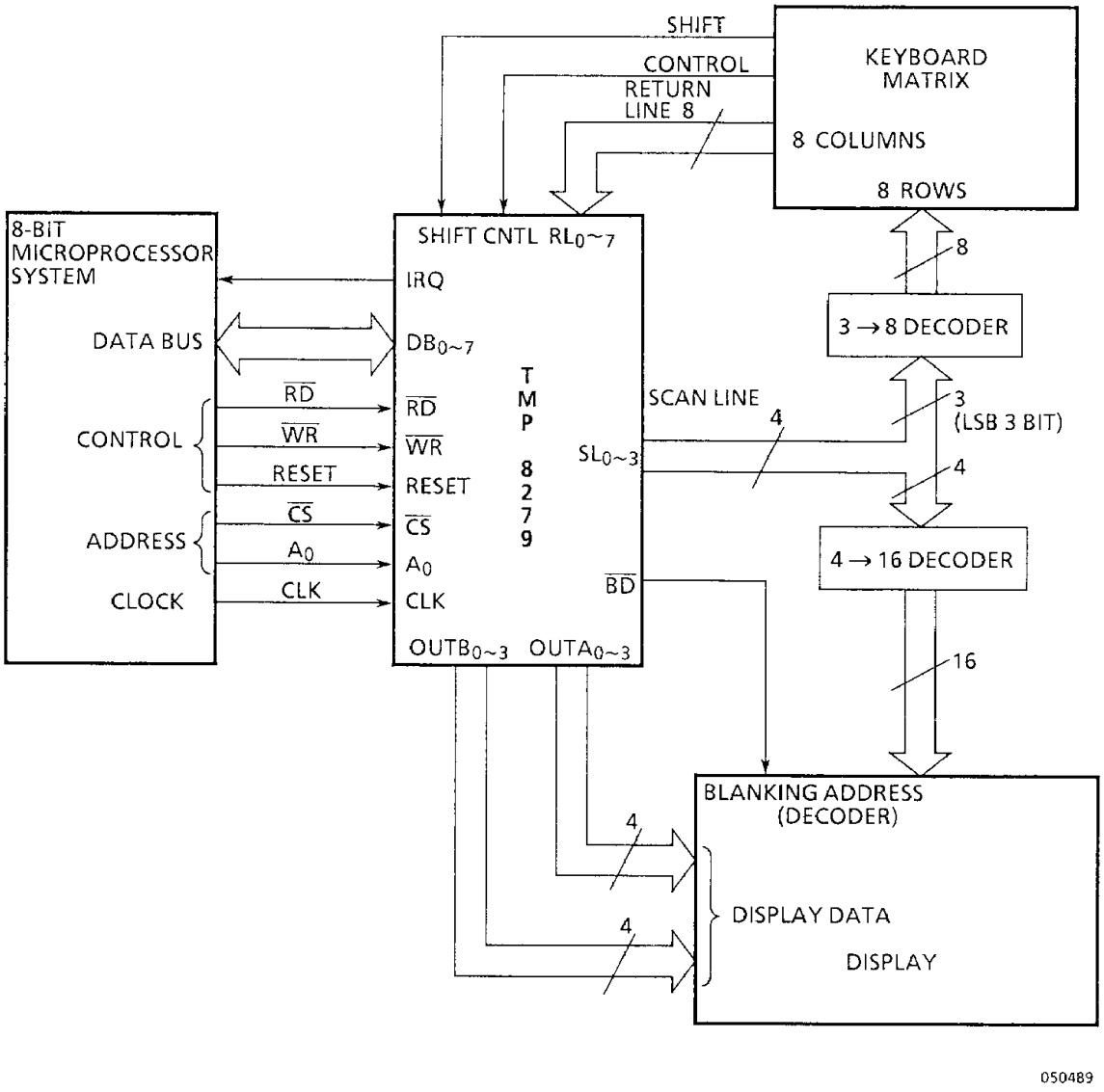

Figure 14.1 Example of Application Circuit