INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT153Dual 4-input multiplexer

Product specification
File under Integrated Circuits, IC06

December 1990





74HC/HCT153

FEATURES

- Non-inverting output
- · Separate enable for each output
- · Common select inputs
- See '253" for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- · Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active LOW output enable inputs ($1\overline{E}$, $2\overline{E}$) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The "153" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1 .

The logic equations for the outputs are:

$$\begin{aligned} 1 Y &= 1 \overline{E}. (1I_0.\overline{S}_1.\overline{S}_0 + 1I_1.\overline{S}_1.S_0 + \\ &+ 1I_2.S_1.\overline{S}_0 + 1I_3.S_1.S_0) \end{aligned}$$

$$2Y = 2\overline{E}.(2I_0.\overline{S}_1.\overline{S}_0 + 2I_1.\overline{S}_1.S_0 + 2I_2.S_1.\overline{S}_0 + 2I_3.S_1.S_0)$$

The "153" can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The "153" is similar to the "253" but has standard outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \, ^{\circ}\text{C}$; $t_r = t_f = 6 \, \text{ns}$

SYMBOL	DADAMETED	CONDITIONS	TYP	LINUT	
	PARAMETER	CONDITIONS	НС	нст	UNIT
t _{PHL} / t _{PLH}	propagation delay	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$			
	1I _n , 2I _n to nY		14	16	ns
	S _n to nY		15	17	ns
	nE to nY		10	11	ns
Cı	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

f_i = input frequency in MHz

f_o = output frequency in MHz

 C_L = output load capacitance in pF

 V_{CC} = supply voltage in V

 $\sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$

2. For HC the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

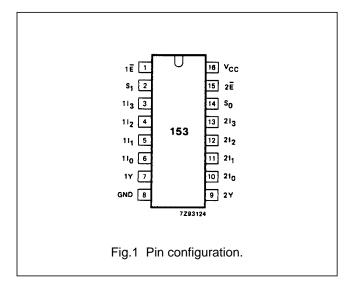
ORDERING INFORMATION

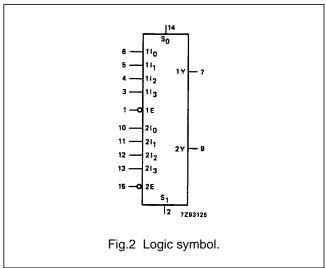
See "74HC/HCT/HCU/HCMOS Logic Package Information".

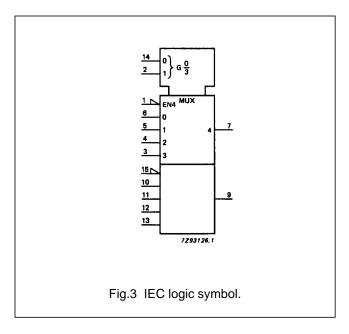
74HC/HCT153

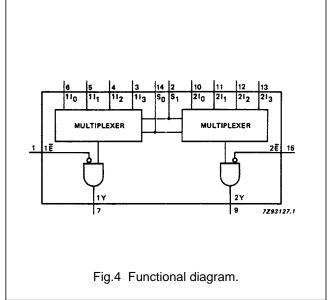
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	1E, 2E	output enable inputs (active LOW)
14, 2	S ₀ , S ₁	common data select inputs
6, 5, 4, 3	1I ₀ to 1I ₃	data inputs from source 1
7	1Y	multiplexer output from source 1
8	GND	ground (0 V)
9	2Y	multiplexer output from source 2
10, 11, 12, 13	2l ₀ to 2l ₃	data inputs from source 2
16	V _{CC}	positive supply voltage









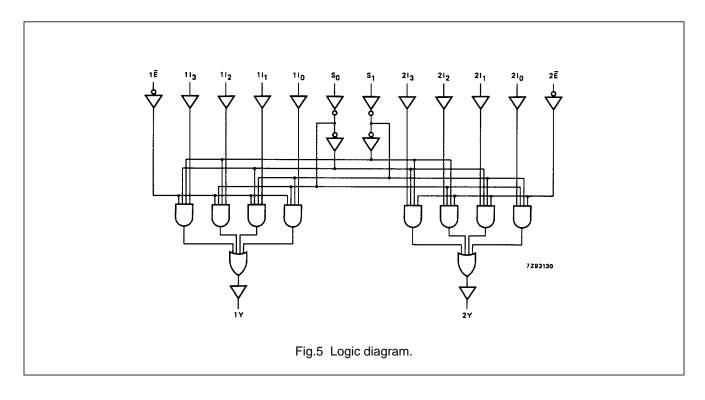
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FUNCTION TABLE

SELECT INPUTS			DATA I	NPUTS	OUTPUT ENABLE	OUTPUT	
S ₀	S ₁	nl ₀	nl ₁	nl ₂	nl ₃	ηĒ	nY
Х	Х	Х	Х	Х	Х	Н	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	Н
Н	L	X	L	X	X	L	L
Н	L	X	H	X	X	L	H
L	Н	X	X	L	X	L	L
L	H	X	X	H	X	L	Н
Н	Н	X	X	X	L	L	L
Н	H	X	X	X	Н	L	H

Note

- 1. H = HIGH voltage level
 - L = LOW voltage level
 - X = don't care



Philips Semiconductors Product specification

Dual 4-input multiplexer

74HC/HCT153

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									WAVEFORMS
		+25			−40 to+85 −40		-40 t	-40 to+125		V _{CC}	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(-,	
	propagation delay		47	145		180		220		2.0	
t _{PHL} / t _{PLH}	1I _n to nY;		17	29		36		44	ns	4.5	Fig.6
	2I _n to nY		14	25		31		38		6.0	
	propagation delay S _n to nY		50	150		190		225		2.0	
t _{PHL} / t _{PLH}			18	30		38		45	ns	4.5	Fig.7
			14	26		33		38		6.0	
	propagation delay nE to nY		33	100		125		150		2.0	
t _{PHL} / t _{PLH}			12	20		25		30	ns	4.5	Fig.7
			10	17		21		26		6.0	
t _{THL} / t _{TLH}	output transition time		19	75		95		110		2.0	
			7	15		19		22	ns	4.5	Figs 6 and 7
			6	13		16		19		6.0	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT							
1I _n , 2I _n nE	0.45							
nE	0.60							
S _n	1.35							

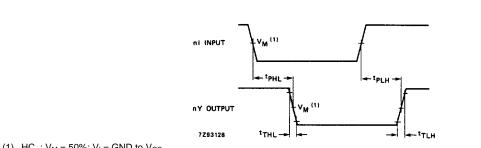
AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL		T _{amb} (°C)							LINIT	TEST CONDITIONS	
	PARAMETER	74НСТ									WAVEFORMS
		+25			−40 to+85		−40 to+125		UNIT	V _{CC} (V)	VVAVEPORIVIS
		min.	typ.	max.	min.	max.	min.	max.		(-,	
t _{PHL}	propagation delay 1I _n to nY; 2I _n to nY		19	34		43		51	ns	4.5	Fig.6
t _{PLH}	propagation delay 1I _n to nY; 2I _n to nY		13	24		30		36	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to nY		20	34		43		51	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay nE to nY		14	27		34		41	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

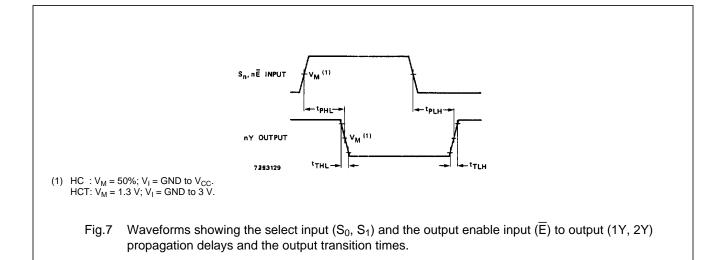
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AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC} . HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig. 6 Waveforms showing the input $(1I_n, 2I_n)$ to output (1Y, 2Y) propagation delays and the output transition times.



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".