

# SN74LS298

## Quad 2-Input Multiplexer with Storage

The SN74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High Speed Termination Effects

### GUARANTEED OPERATING RANGES

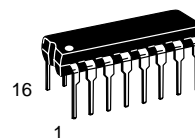
Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			-0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA



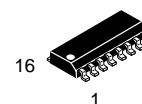
ON Semiconductor™

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**LOW  
POWER  
SCHOTTKY**



PLASTIC  
N SUFFIX  
CASE 648



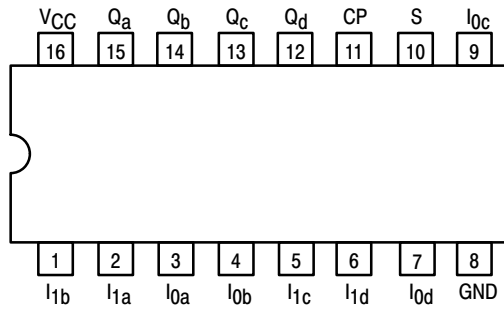
SOIC  
D SUFFIX  
CASE 751B

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS298N	16 Pin DIP	2000 Units/Box
SN74LS298D	SOIC-16	38 Units/Rail
SN74LS298DR2	SOIC-16	2500/Tape & Reel

# SN74LS298

## CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

<u>S</u>	Common Select Input
$\overline{CP}$	Clock (Active LOW Going Edge) Input
$I_{0a} - I_{0d}$	Data Inputs from Source 0
$I_{1a} - I_{1d}$	Data Inputs from Source 1
$Q_a - Q_d$	Register Outputs

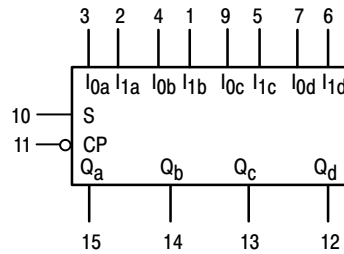
### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

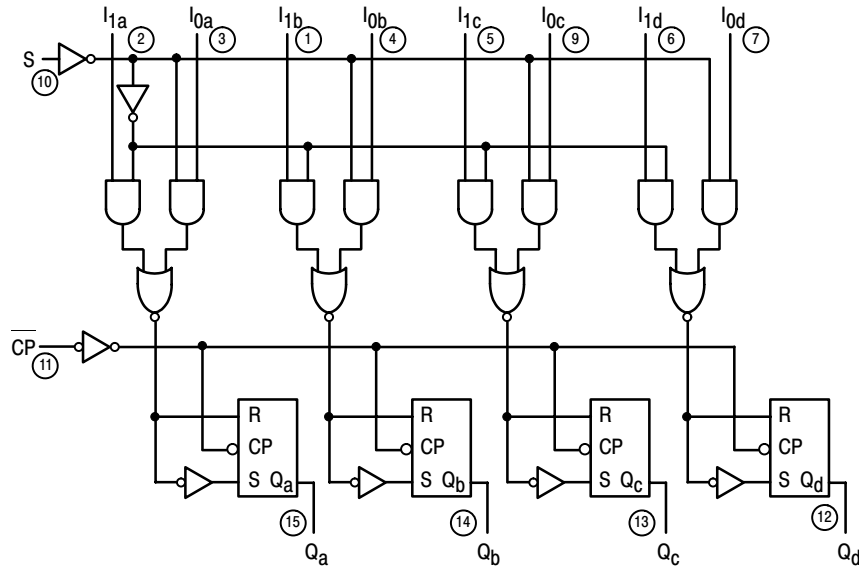
### LOGIC SYMBOL



$V_{CC}$  = PIN 16  
GND = PIN 8

# SN74LS298

## LOGIC OR BLOCK DIAGRAM



$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

### FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW transition of the Clock input (CP). The 4-bit

output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

### TRUTH TABLE

INPUTS			OUTPUT
S	I <sub>0</sub>	I <sub>1</sub>	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level  
 H = HIGH Voltage Level  
 X = Don't Care  
 l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.  
 h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
			0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current			21	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub>	Propagation Delay, Clock to Output		18	27	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 15 pF
t <sub>PHL</sub>			21	32	ns	

## AC SET-UP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>S</sub>	Data Setup Time	15			ns	
t <sub>S</sub>	Select Setup Time	25			ns	
t <sub>H</sub>	Data Hold Time	5.0			ns	
t <sub>H</sub>	Select Hold Time	0				

## DEFINITIONS OF TERMS

SETUP TIME (t<sub>S</sub>) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t<sub>H</sub>) — is defined as the minimum time following the clock transition from LOW to HIGH that the

logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

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## AC WAVEFORMS

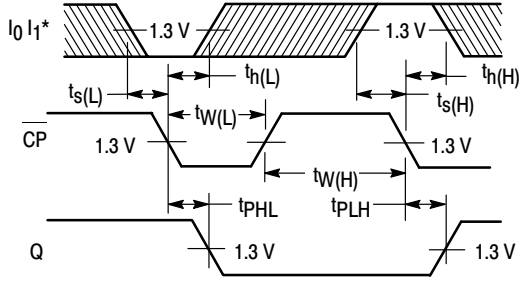


Figure 1.

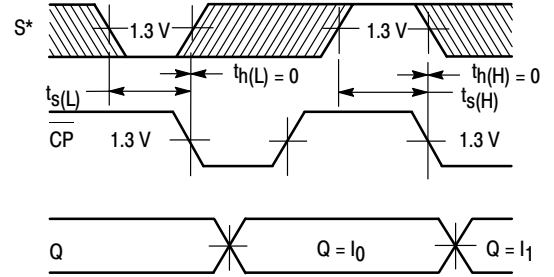


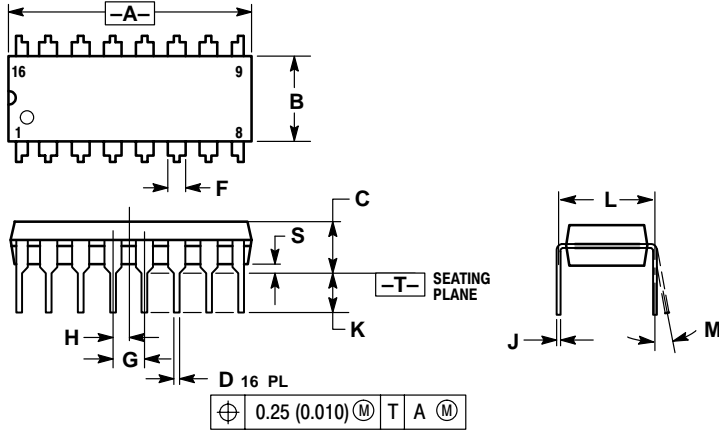
Figure 2.

\*The shaded areas indicate when the input is permitted to change for predictable output performance.

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## PACKAGE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
**CASE 648-08**  
**ISSUE R**



**NOTES:**

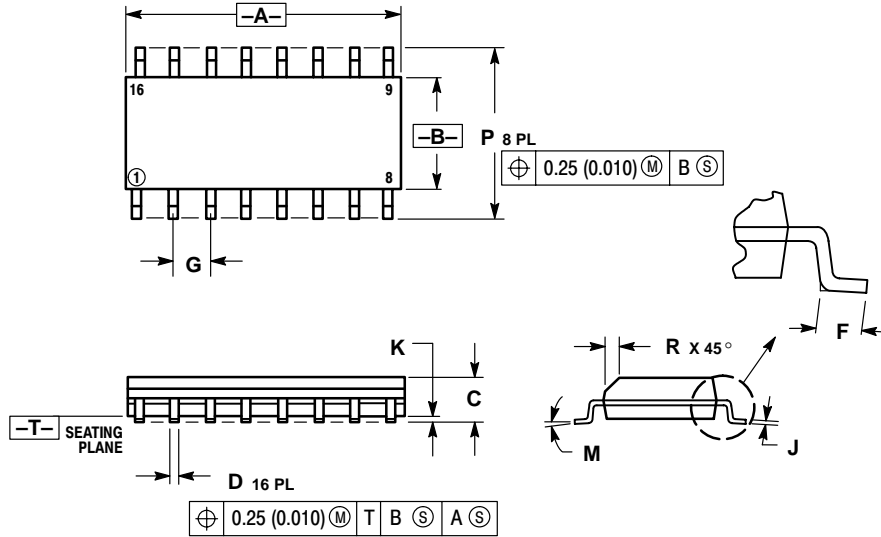
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

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## PACKAGE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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