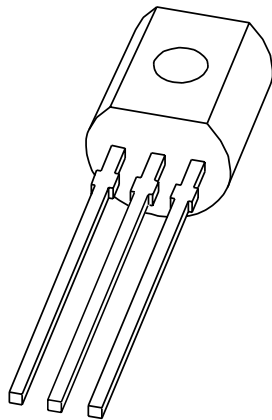


# DATA SHEET



## **2N5400; 2N5401** **PNP high-voltage transistors**

Product specification  
Supersedes data of September 1994  
File under Discrete Semiconductors, SC04

1997 May 22

# PNP high-voltage transistors

# 2N5400; 2N5401

### FEATURES

- Low current (max. 300 mA)
- High voltage (max. 150 V).

### APPLICATIONS

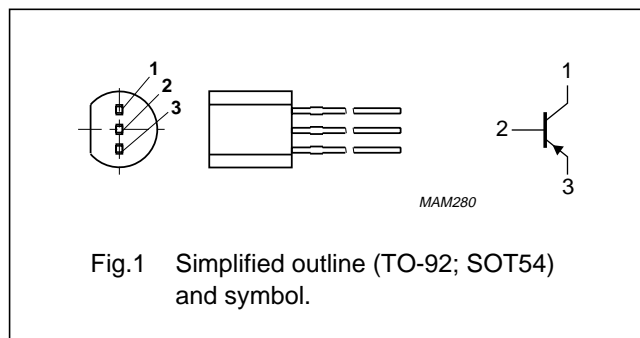
- General purpose switching and amplification
- Telephony applications.

### DESCRIPTION

PNP high-voltage transistor in a TO-92; SOT54 plastic package. NPN complements: 2N5550 and 2N5551.

### PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter			
	2N5400		–	–130	V
	2N5401		–	–160	V
V <sub>CEO</sub>	collector-emitter voltage	open base			
	2N5400		–	–120	V
	2N5401		–	–150	V
I <sub>CM</sub>	peak collector current		–	–600	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	–	630	mW
h <sub>FE</sub>	DC current gain	I <sub>C</sub> = 10 mA; V <sub>CE</sub> = –5 V			
	2N5400		40	–	
	2N5401		60	–	
f <sub>T</sub>	transition frequency	I <sub>C</sub> = –10 mA; V <sub>CE</sub> = –10 V; f = 100 MHz			
	2N5400		100	400	MHz
	2N5401		100	300	MHz

## PNP high-voltage transistors

2N5400; 2N5401

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter			
	2N5400		–	–130	V
	2N5401		–	–160	V
V <sub>CEO</sub>	collector-emitter voltage	open base			
	2N5400		–	–120	V
	2N5401		–	–150	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	–5	V
I <sub>C</sub>	collector current (DC)		–	–300	mA
I <sub>CM</sub>	peak collector current		–	–600	mA
I <sub>BM</sub>	peak base current		–	–100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	–	630	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1	200	K/W

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

## PNP high-voltage transistors

## 2N5400; 2N5401

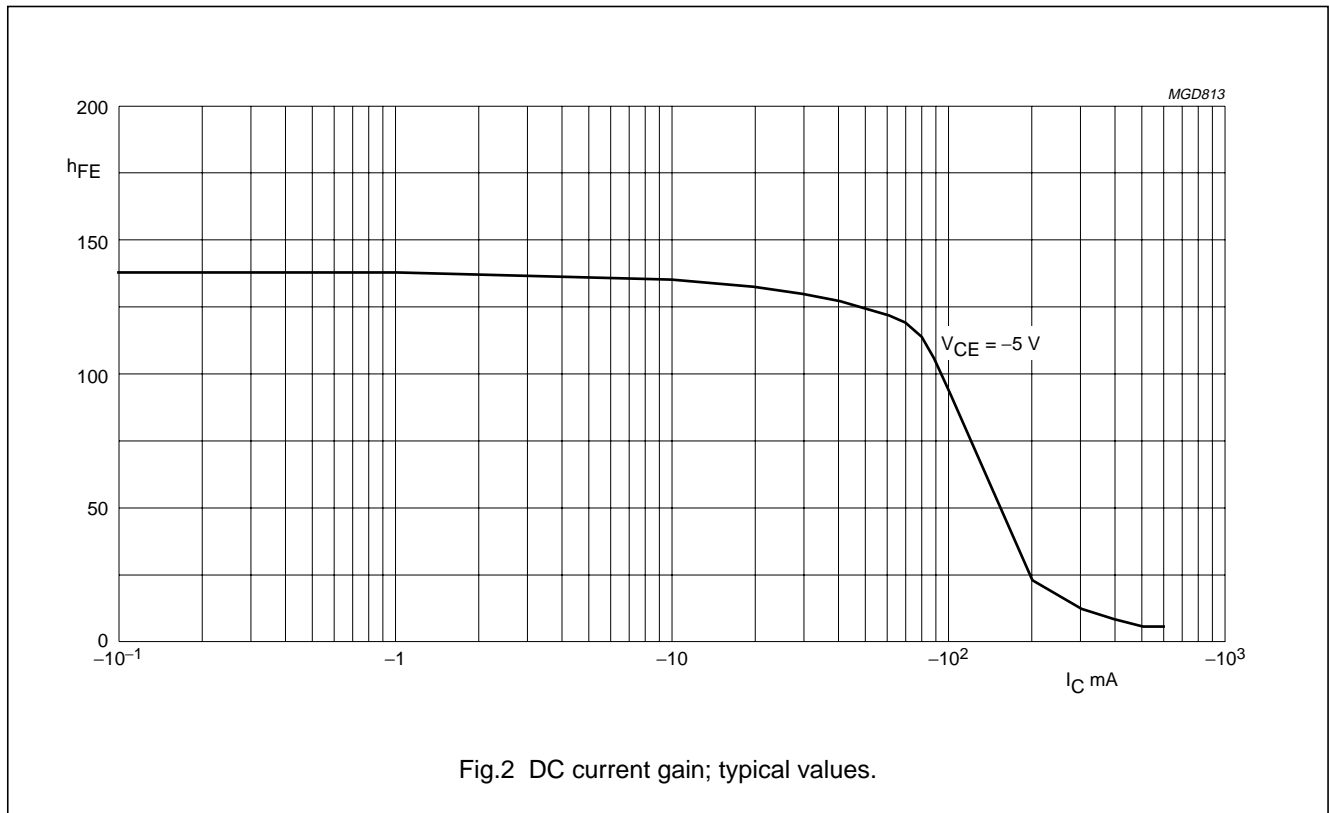
**CHARACTERISTICS**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector cut-off current 2N5400	$I_E = 0; V_{CB} = -100\text{ V}$	–	–100	nA
		$I_E = 0; V_{CB} = -100\text{ V}; T_{amb} = 100\text{ °C}$	–	–100	$\mu\text{A}$
$I_{CBO}$	collector cut-off current 2N5401	$I_E = 0; V_{CB} = -120\text{ V}$	–	–50	nA
		$I_E = 0; V_{CB} = -120\text{ V}; T_{amb} = 100\text{ °C}$	–	–50	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = -4\text{ V}$	–	–50	nA
$h_{FE}$	DC current gain 2N5400 2N5401	$I_C = -1\text{ mA}; V_{CE} = -5\text{ V};$ see Fig.2	30	–	
			50	–	
$h_{FE}$	DC current gain 2N5400 2N5401	$I_C = -10\text{ mA}; V_{CE} = -5\text{ V};$ see Fig.2	40	180	
			60	240	
$h_{FE}$	DC current gain 2N5400 2N5401	$I_C = -50\text{ mA}; V_{CE} = -5\text{ V};$ see Fig.2	40	–	
			50	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -1\text{ mA}$	–	–200	mV
		$I_C = -50\text{ mA}; I_B = -5\text{ mA}$	–	–500	mV
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = -10\text{ V}; f = 1\text{ MHz}$	–	6	pF
$f_T$	transition frequency 2N5400 2N5401	$I_C = -10\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	100	400	MHz
			100	300	MHz
F	noise figure	$I_C = -200\text{ }\mu\text{A}; V_{CE} = -5\text{ V}; R_S = 2\text{ k}\Omega;$ $f = 10\text{ Hz to }15.7\text{ kHz}$	–	8	pF

PNP high-voltage transistors

2N5400; 2N5401



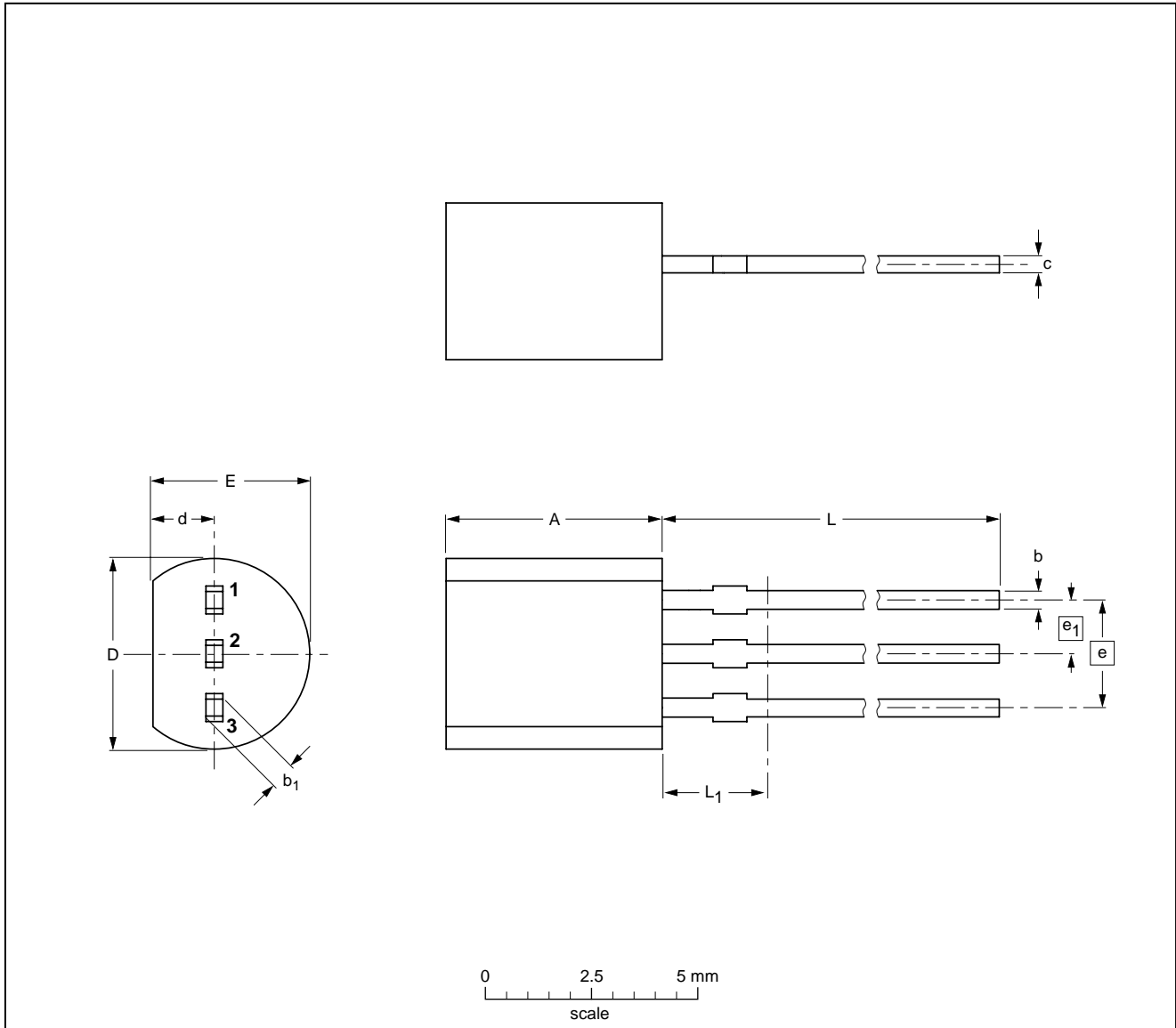
PNP high-voltage transistors

2N5400; 2N5401

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54		TO-92	SC-43		97-02-28

## PNP high-voltage transistors

2N5400; 2N5401

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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